192 Bits Thermal Printer Head Driver

GENERAL DESCRIPTION

FS9140S is a 192-bit CMOS driver for thermal printer head. It includes 192 built-in shift registers to transfer the data, and 192 latches to hold the input data. In general, “H” or “L” levels can be selected for driver enable. Latch operation control depends on LATX_X (LATX_L/ LATX_R), driver output control depends on STB_X (STB_L/ STB_R).

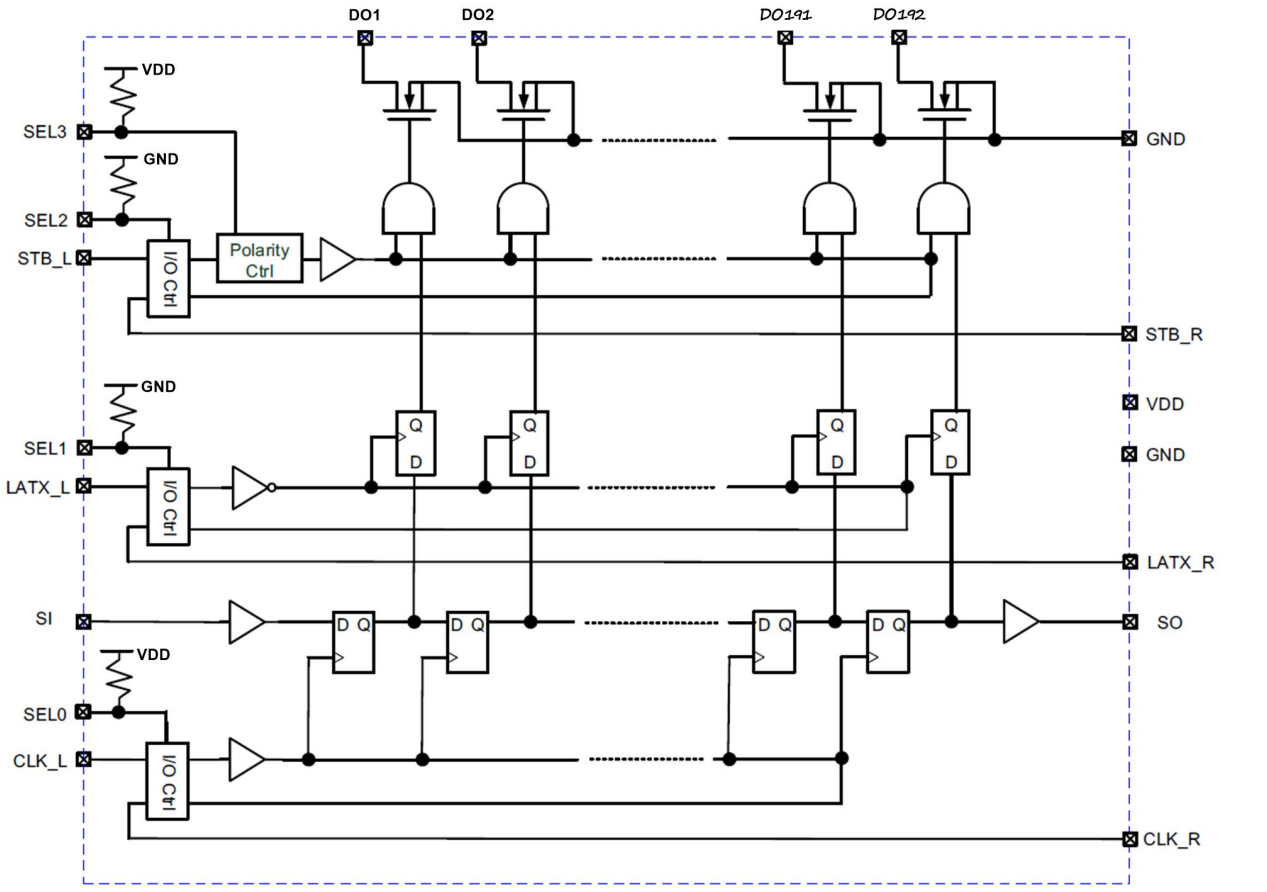
FEATURES

- Low current consumption : 1mA@ typical case (VDD=3.3V, fclk=10MHz, SI : high/low fixed)
- High speed operation: 20MHz @ VDD(min) = 3.0V
- Driver output voltage : up to 24V
- Driver output current : 80mA max.
- Built-in 192-bit register and latch
- Enable control
- Rdson: < 2.0 Ohm

APPLICATIONS

- Thermal printer head

FUNCTIONAL BLOCK DIAGRAM



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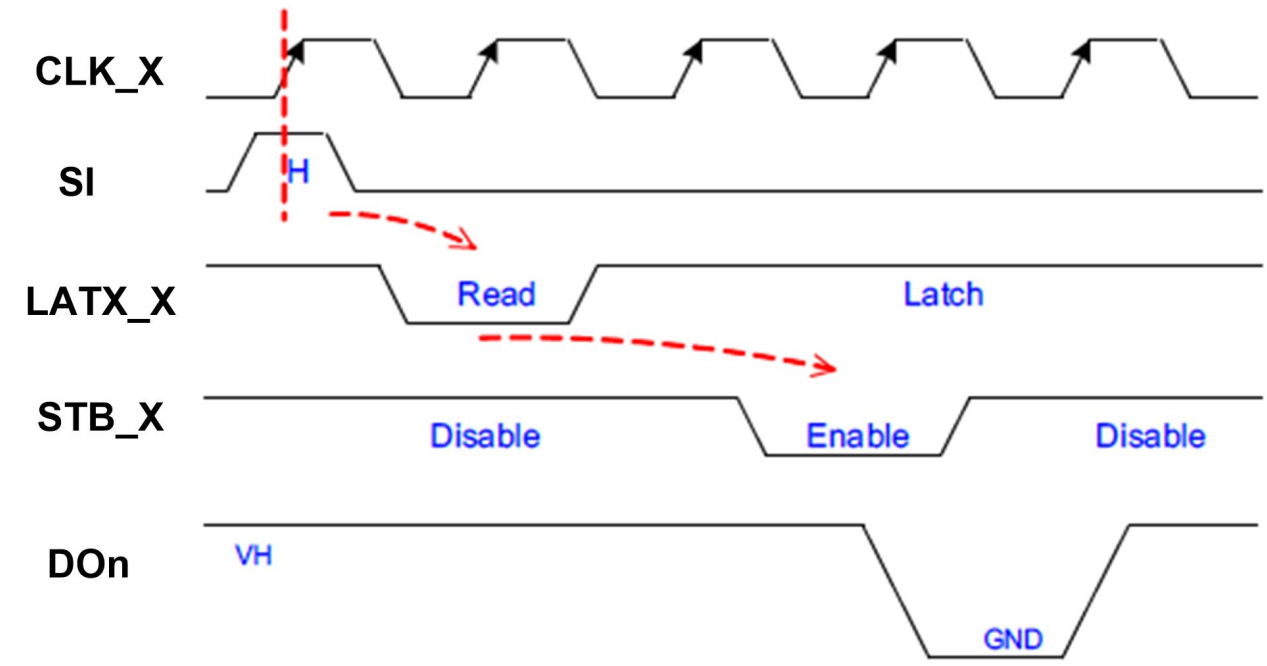
Operation Description

The 192-bit shift register reads the data input from SI on the rising edge of the CLK_X (CLK_L/CLK_R) input. The operation of latch circuit depends on the level of LATX_X ; it reads the data of the shift register when its LATX_X is low and it holds the data of the shift register when the level is different. The latch data is output to the respective output drivers when STB_X is Low and SEL3 is high, or when STB_X is high and SEL3 is low. Turning STB_X high when SEL3 is high or turing STB_X low when SEL3 is low makes all driver output transistors go off. The operation and relationship of these control signals when SEL3 = High are shown as followings.



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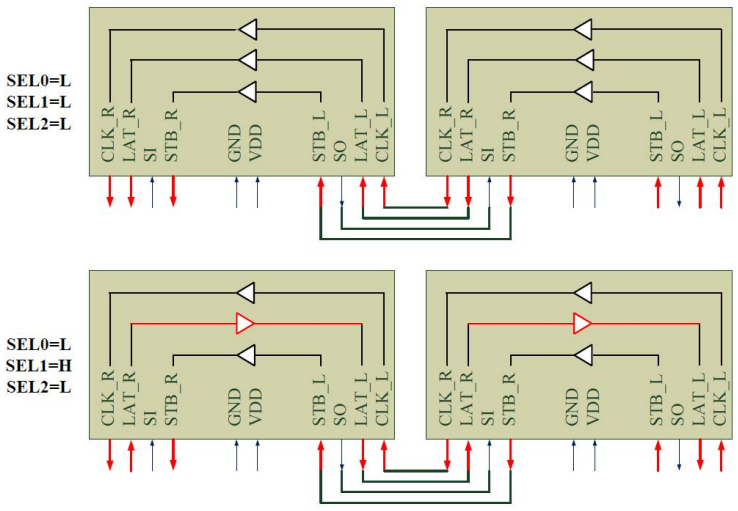
PAD Information

PAD Name	I/O	Description
SI	I	Serial data input for 192-bit shift register
SO	O	Serial data output for 192-bit shift register
CLK_R/CLK_L	I/O	Clock input
LATX_R/LATX_L	I/O	Data latch signal control, with pull-up resistor: 1. When LATX= “H”: holds the preceding data 2. When LATX= “L”: reads the data of the shift register
STB_R STB_L	I/O I/O	Driver enable level control 1. When SEL3 = H, STB with pull-up resistor DO outputs when STB is L, DO is high impedance when STB is H 2. When SEL3 = L, STB with pull-down resistor DO outputs when STB is H, DO is high impedance when STB is L
SEL0, SEL1, SEL2	I I	Signal direction control, SEL0 with pull-up resistor, SEL1/2 with pull-down resistor SEL0 for CLK control, SEL1 for LATX control and SEL2 for STB control
SEL3	I	STB polarity control and SEL3 with pull-up resistor
VDD		Positive power supply for logic function (2.6V~5.5V)
GND		Ground for logic function and driver(number :96)
DO1-DO192	O	Driver outputs (open-drained NMOS)



SEL0, SEL1 and SEL2 are used to control signal direction:

- CLK_L is input and CLK_R is output when SEL0 is L
- LATX_L is input and LATX_R is output when SEL1 is L
- STB_L is input and STB_R is output when SEL2 is L.

The SEL0/1 operation are shown on the left.

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ABSOLUTE MAXIMUM RATINGS

VDD to GND Voltage	-0.4V ~ 7V
DO1, DO2…DO192 to GND Voltage	-0.4V ~ 35V
DO1, DO2…DO192 Output Current	MAX 80mA
STB_X, LATX_X, SI, CLK_X,SEL0..SEL3 to GND Voltage	-0.5V ~ VDD+0.5V
STB_X, LATX_X, SI, CLK_X,SEL0..SEL3 Input Current	-20mA ~ 20mA
SO, CLK_X,LATX_X to GND Voltage	-0.5V ~ VDD+0.5V
Operating temperature range, T_J	-25°C~85°C
Storage temperature range, T_{STG}	-65°~+150°C

Note:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		2.6	3.3	5.5	V
High level Input Voltage	V_{IN}		0.7V_{DD}			V
Low level Input Voltage	V_{IL}				0.3V_{DD}	V
High level Input Current	I_{IH}	Except SEL1/2 (SEL3=H)			1	uA
	I_{IH}	Pins for STB_X, SEL1/2 (SEL3=L)			40	uA
Low level Input Current	I_{IL}	Pins for STB_X, SEL1/2 (SEL3=L)			1	uA
	I_{IL}	SEL1/2 (SEL3=H)	`		40	uA
High level driver output voltage	V_{DOH}				24	V
Low level driver output voltage	V_{DDL}	VDD=3.0V,IDOL=50mA		0.1	0.2	V
		VDD=5.0V,IDOL=50mA		0.09	0.18	
		VDD=3.0V,IDOL=30mA		0.06	0.12	
		VDD=5.0V,IDOL=30mA		0.055	0.11	
Driver Output Current	I_{DOL}				80	mA
Driver Leakage Current	I_{LEAK}	VDOH=24V for 1-dot output			1	uA
Current Consumption VDD=3.3V,fclk=10MHz,	I_{VDD}	SI : high fixed		1	2	mA
		SI : 1/2 fclk		1.5	3	mA
Standby Current (Ta = 85℃)	I_{STB}	VDD = 2.6V ~ 5.5V			10	uA
Input Capacitance	C_{IN}			5	10	pF

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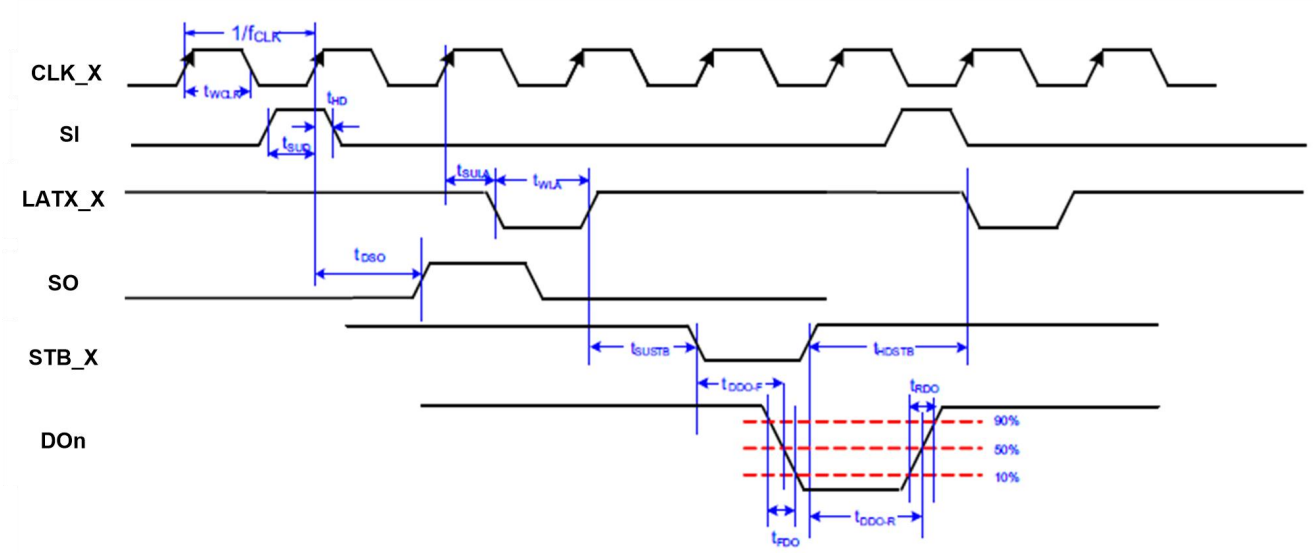
AC ELECTRICAL CHARACTERISTICS



(VDD=2.6~4.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency (cascade)	f_{CLK}	V_{DD}=3.0V			20	MHz
Clock pulse width	t_{WCLK}	V_{DD}=3.0V, f_{clk}=20MHz	10			ns
Data setup time	t_{SUD}	V_{DD}=3.0V, f_{clk}=20MHz	10			ns
Data hold time	t_{HD}	V_{DD}=3.0V, f_{clk}=20MHz	10			ns
Latch pulse width	t_{WLA}	V_{DD}=3.0V, f_{clk}=20MHz	10			ns
Latch setup time	t_{SULA}	V_{DD}=3.0V, f_{clk}=20MHz	10			ns
STB_X – LATX_X setup time	t_{SUSTB}	V_{DD}=3.0V, f_{clk}=20MHz	300			ns
STB_X – LATX_X hold time	t_{HDSTB}	V_{DD}=3.0V, f_{clk}=20MHz	15			us
CLK_X-SO propagation delay time	t_{DSO}	V_{DD}=3.0V, f_{clk}=20MHz,C_L=5pF	3		40	ns
STB_X -DOn rising enable delay time	t_{DDO-R}	V_{DD}=3.0V, RL=200Ω, V_H=24V, C_L=5pF		10	20	us
STB_X -DOn falling enable delay time	t_{DDO-F}	V_{DD}=3.0V, RL=200Ω, V_H=24V, C_L=5pF		5	10	us
DOn rising time	t_{RDO}	V_{DD}=3.0V, RL=200Ω, V_H=24V, C_L=5pF		10	20	us
DOn falling time	t_{FDO}	V_{DD}=3.0V, RL=200Ω, V_H=24V, C_L=5pF		5	10	us

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CLK input to output delay time	t_{DCLK}		2		10	ns
LAT input to output delay time	t_{DLAT}		2		10	ns
STB input to output delay time	t_{DSTB}		2		10	ns

(VDD=4.5~5.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency (cascade)	f_{CLK}	V_{DD}=5.0V			30	MHz
Clock pulse width	t_{WCLK}	V_{DD}=5.0V, f_{clk}=30MHz	10			ns
Data setup time	t_{SUD}	V_{DD}=5.0V, f_{clk}=30MHz	10			ns
Data hold time	t_{HD}	V_{DD}=5.0V, f_{clk}=30MHz	10			ns
Latch pulse width	t_{WLA}	V_{DD}=5.0V, f_{clk}=30MHz	10			ns
Latch setup time	t_{SULA}	V_{DD}=5.0V, f_{clk}=30MHz	10			ns
STB_X – LATX_X setup time	t_{SUSTB}	V_{DD}=5.0V, f_{clk}=30MHz	300			ns
STB_X – LATX_X hold time	t_{HDSTB}	V_{DD}=5.0V, f_{clk}=30MHz	13			us
CLK_X-SO propagation delay time	t_{DSO}	V_{DD}=5.0V, f_{clk}=30MHz,C_L=5pF	3		30	ns
STB_X-DOn rising enable delay time	t_{DDO-R}	V_{DD}=5.0V, RL=200Ω, V_H=24V, C_L=5pF		10	20	us
STB_X -DOn falling enable delay time	t_{DDO-F}	V_{DD}=5.0V, RL=200Ω, V_H=24V, C_L=5pF		5	10	us
DOn rising time	t_{RDO}	V_{DD}=5.0V, RL=200Ω, V_H=24V, C_L=5pF		10	20	us
DOn falling time	t_{FDO}	V_{DD}=5.0V, RL=200Ω, V_H=24V, C_L=5pF		5	10	us
CLK input to output delay time	t_{DCLK}		2		10	ns
LAT input to output delay time	t_{DLAT}		2		10	ns
STB input to output delay time	t_{DSTB}		2		10	ns

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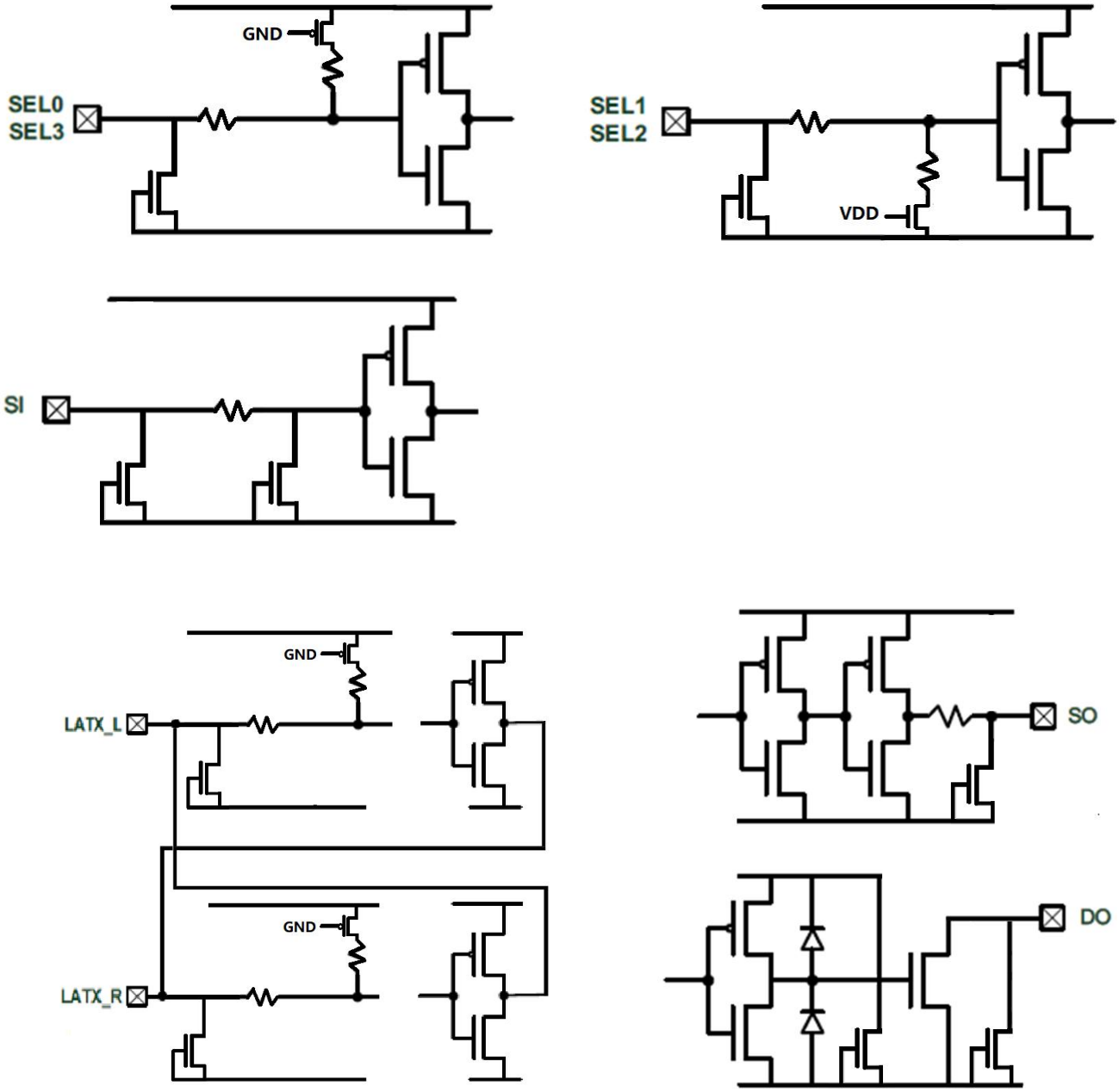
ESD Architecture



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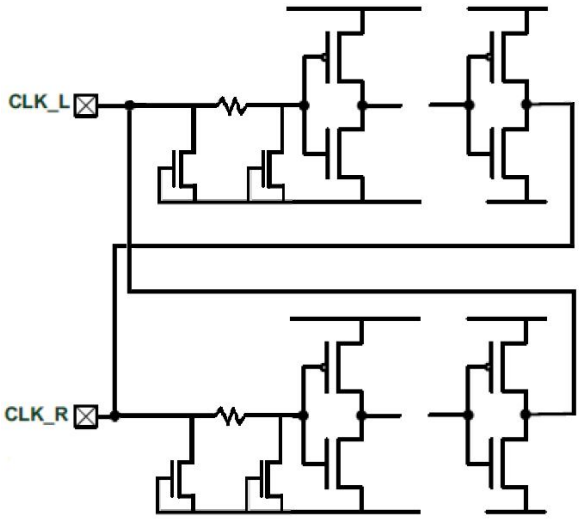

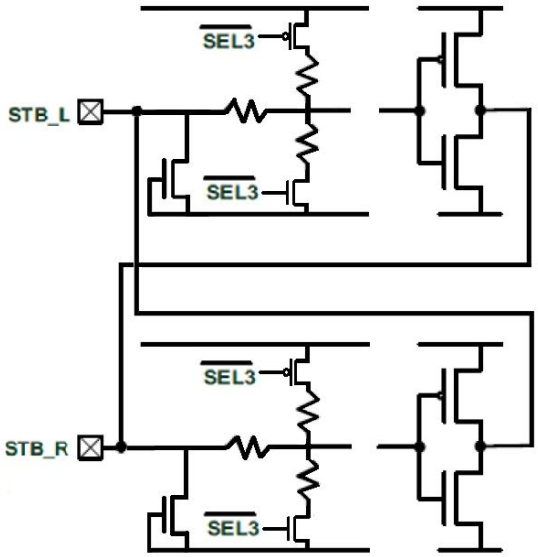

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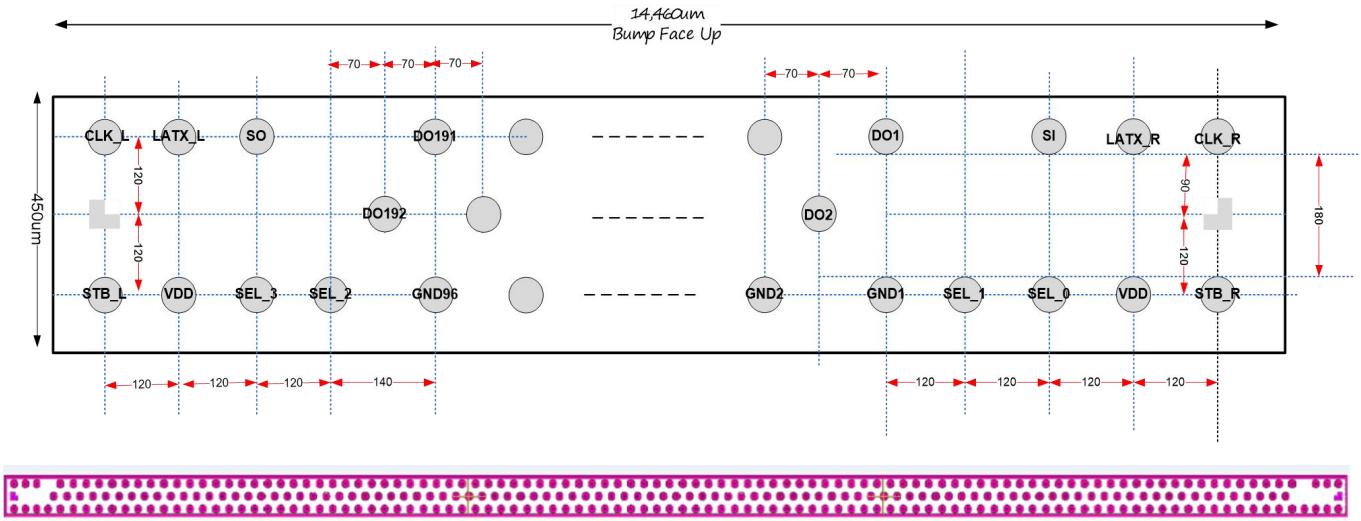
Dimensions and Pad Configuration



Chip thickness : 300 ± 30 um

Chip size : 14,460um X 450um including 60um scribe line

Solder Ball Diameter: 68um

DOn pad pitch: 70um

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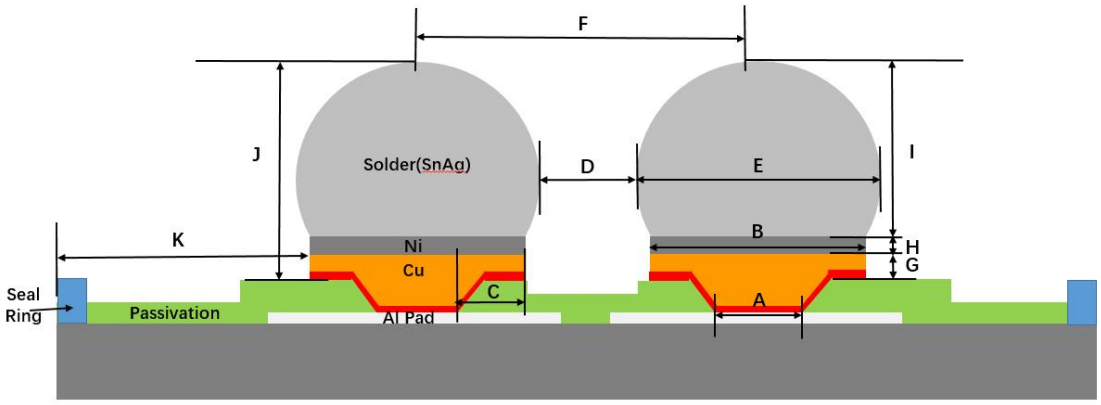
Solder Ball Configuration



Item	Description
UBM Structure	Sputtering Ti(1000A)/Cu (3000A)
Bump Material	Cu + Ni+Sn/1.8%Ag by plating

Item	Description	Specification（um）
A	Passivation opening	50
B	UBM size	64
C	Passivation opening to bump edge	7
D	Bump space	52
E	Bump diameter(post reflow)	68
F	Bump pitch	120
G	Cu height	5
H	Ni height	3
I	Solder cap height(post reflow)	40
J	Total bump height(post reflow)	48
K	Bump edge to seal ring inner edge	>20
	Bump Height Coplanarity (Within Die)	<10

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Pad Coordinates

(The origin of the coordinates axes is the center of the chip) unit : (um)

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	CLK_L	-7139	120	102	GND90	-5799	-120	203	DO95	81	120
2	CLK_R	7141	120	103	GND91	-5939	-120	204	DO96	11	0
3	SEL_3	-6899	-120	104	GND92	-6079	-120	205	DO97	-59	120
4	SEL_0	6901	-120	105	GND93	-6219	-120	206	DO98	-129	0
5	SEL_2	-6779	-120	106	GND94	-6359	-120	207	DO99	-199	120
6	SEL_1	6781	-120	107	GND95	-6499	-120	208	DO100	-269	0
7	STB_L	-7139	-120	108	GND96	-6639	-120	209	DO101	-339	120
8	STB_R	7141	-120	109	DO1	6661	120	210	DO102	-409	0
9	LATX_L	-7019	120	110	DO2	6591	0	211	DO103	-479	120
10	LATX_R	7021	120	111	DO3	6521	120	212	DO104	-549	0
11	SO	-6899	120	112	DO4	6451	0	213	DO105	-619	120
12	SI	6901	120	113	DO5	6381	120	214	DO106	-689	0
13	GND1	6661	-120	114	DO6	6311	0	215	DO107	-759	120
14	GND2	6521	-120	115	DO7	6241	120	216	DO108	-829	0
15	GND3	6381	-120	116	DO8	6171	0	217	DO109	-899	120
16	GND4	6241	-120	117	DO9	6101	120	218	DO110	-969	0
17	GND5	6101	-120	118	DO10	6031	0	219	DO111	-1039	120
18	GND6	5961	-120	119	DO11	5961	120	220	DO112	-1109	0
19	GND7	5821	-120	120	DO12	5891	0	221	DO113	-1179	120
20	GND8	5681	-120	121	DO13	5821	120	222	DO114	-1249	0
21	GND9	5541	-120	122	DO14	5751	0	223	DO115	-1319	120
22	GND10	5401	-120	123	DO15	5681	120	224	DO116	-1389	0
23	GND11	5261	-120	124	DO16	5611	0	225	DO117	-1459	120
24	GND12	5121	-120	125	DO17	5541	120	226	DO118	-1529	0
25	GND13	4981	-120	126	DO18	5471	0	227	DO119	-1599	120
26	GND14	4841	-120	127	DO19	5401	120	228	DO120	-1669	0
27	GND15	4701	-120	128	DO20	5331	0	229	DO121	-1739	120
28	GND16	4561	-120	129	DO21	5261	120	230	DO122	-1809	0
29	GND17	4421	-120	130	DO22	5191	0	231	DO123	-1879	120
30	GND18	4281	-120	131	DO23	5121	120	232	DO124	-1949	0
31	GND19	4141	-120	132	DO24	5051	0	233	DO125	-2019	120
32	GND20	4001	-120	133	DO25	4981	120	234	DO126	-2089	0
33	GND21	3861	-120	134	DO26	4911	0	235	DO127	-2159	120
34	GND22	3721	-120	135	DO27	4841	120	236	DO128	-2229	0
35	GND23	3581	-120	136	DO28	4771	0	237	DO129	-2299	120

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36	GND24	3441	-120	**137**	D029	4701	120	**238**	D0130	-2369	0
37	GND25	3301	-120	**138**	D030	4631	0	**239**	D0131	-2439	120
38	GND26	3161	-120	**139**	D031	4561	120	**240**	D0132	-2509	0
39	GND27	3021	-120	**140**	D032	4491	0	**241**	D0133	-2579	120
40	GND28	2881	-120	**141**	D033	4421	120	**242**	D0134	-2649	0
41	GND29	2741	-120	**142**	D034	4351	0	**243**	D0135	-2719	120
42	GND30	2601	-120	**143**	D035	4281	120	**244**	D0136	-2789	0
43	GND31	2461	-120	**144**	D036	4211	0	**245**	D0137	-2859	120
44	GND32	2321	-120	**145**	D037	4141	120	**246**	D0138	-2929	0
45	GND33	2181	-120	**146**	D038	4071	0	**247**	D0139	-2999	120
46	GND34	2041	-120	**147**	D039	4001	120	**248**	D0140	-3069	0
47	GND35	1901	-120	**148**	D040	3931	0	**249**	D0141	-3139	120
48	GND36	1761	-120	**149**	D041	3861	120	**250**	D0142	-3209	0
49	GND37	1621	-120	**150**	D042	3791	0	**251**	D0143	-3279	120
50	GND38	1481	-120	**151**	D043	3721	120	**252**	D0144	-3349	0
51	GND39	1341	-120	**152**	D044	3651	0	**253**	D0145	-3419	120
52	GND40	1201	-120	**153**	D045	3581	120	**254**	D0146	-3489	0
53	GND41	1061	-120	**154**	D046	3511	0	**255**	D0147	-3559	120
54	GND42	921	-120	**155**	D047	3441	120	**256**	D0148	-3629	0
55	GND43	781	-120	**156**	D048	3371	0	**257**	D0149	-3699	120
56	GND44	641	-120	**157**	D049	3301	120	**258**	D0150	-3769	0
57	GND45	501	-120	**158**	D050	3231	0	**259**	D0151	-3839	120
58	GND46	361	-120	**159**	D051	3161	120	**260**	D0152	-3909	0
59	GND47	221	-120	**160**	D052	3091	0	**261**	D0153	-3979	120
60	GND48	81	-120	**161**	D053	3021	120	**262**	D0154	-4049	0
61	GND49	-59	-120	**162**	D054	2951	0	**263**	D0155	-4119	120
62	GND50	-199	-120	**163**	D055	2881	120	**264**	D0156	-4189	0
63	GND51	-339	-120	**164**	D056	2811	0	**265**	D0157	-4259	120
64	GND52	-479	-120	**165**	D057	2741	120	**266**	D0158	-4329	0
65	GND53	-619	-120	**166**	D058	2671	0	**267**	D0159	-4399	120
66	GND54	-759	-120	**167**	D059	2601	120	**268**	D0160	-4469	0
67	GND55	-899	-120	**168**	D060	2531	0	**269**	D0161	-4539	120
68	GND56	-1039	-120	**169**	D061	2461	120	**270**	D0162	-4609	0
69	GND57	-1179	-120	**170**	D062	2391	0	**271**	D0163	-4679	120
70	GND58	-1319	-120	**171**	D063	2321	120	**272**	D0164	-4749	0
71	GND59	-1459	-120	**172**	D064	2251	0	**273**	D0165	-4819	120
72	GND60	-1599	-120	**173**	D065	2181	120	**274**	D0166	-4889	0
73	GND61	-1739	-120	**174**	D066	2111	0	**275**	D0167	-4959	120

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74	GND62	-1879	-120	**175**	DO67	2041	120	**276**	DO168	-5029	0
75	GND63	-2019	-120	**176**	DO68	1971	0	**277**	DO169	-5099	120
76	GND64	-2159	-120	**177**	DO69	1901	120	**278**	DO170	-5169	0
77	GND65	-2299	-120	**178**	DO70	1831	0	**279**	DO171	-5239	120
78	GND66	-2439	-120	**179**	DO71	1761	120	**280**	DO172	-5309	0
79	GND67	-2579	-120	**180**	DO72	1691	0	**281**	DO173	-5379	120
80	GND68	-2719	-120	**181**	DO73	1621	120	**282**	DO174	-5449	0
81	GND69	-2859	-120	**182**	DO74	1551	0	**283**	DO175	-5519	120
82	GND70	-2999	-120	**183**	DO75	1481	120	**284**	DO176	-5589	0
83	GND71	-3139	-120	**184**	DO76	1411	0	**285**	DO177	-5659	120
84	GND72	-3279	-120	**185**	DO77	1341	120	**286**	DO178	-5729	0
85	GND73	-3419	-120	**186**	DO78	1271	0	**287**	DO179	-5799	120
86	GND74	-3559	-120	**187**	DO79	1201	120	**288**	DO180	-5869	0
87	GND75	-3699	-120	**188**	DO80	1131	0	**289**	DO181	-5939	120
88	GND76	-3839	-120	**189**	DO81	1061	120	**290**	DO182	-6009	0
89	GND77	-3979	-120	**190**	DO82	991	0	**291**	DO183	-6079	120
90	GND78	-4119	-120	**191**	DO83	921	120	**292**	DO184	-6149	0
91	GND79	-4259	-120	**192**	DO84	851	0	**293**	DO185	-6219	120
92	GND80	-4399	-120	**193**	DO85	781	120	**294**	DO186	-6289	0
93	GND81	-4539	-120	**194**	DO86	711	0	**295**	DO187	-6359	120
94	GND82	-4679	-120	**195**	DO87	641	120	**296**	DO188	-6429	0
95	GND83	-4819	-120	**196**	DO88	571	0	**297**	DO189	-6499	120
96	GND84	-4959	-120	**197**	DO89	501	120	**298**	DO190	-6569	0
97	GND85	-5099	-120	**198**	DO90	431	0	**299**	DO191	-6639	120
98	GND86	-5239	-120	**199**	DO91	361	120	**300**	DO192	-6709	0
99	GND87	-5379	-120	**200**	DO92	291	0	**301**	VDD	-7019	-120
100	GND88	-5519	-120	**201**	DO93	221	120	**302**	VDD	7021	-120
101	GND89	-5659	-120	**202**	DO94	151	0				

Align mark : (unit : um)

	Pad Center (X,Y)

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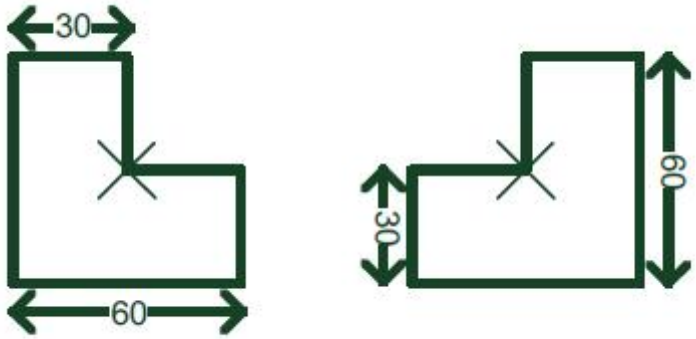
Mark_Left	-7139	0
Mark_Right	7141	0



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