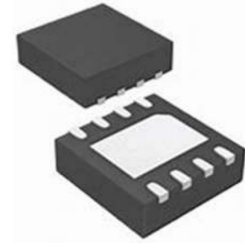


Description

Innotion's YP161515T is a 15 watt, unmatched LDMOS FETs, designed for Wide-band and Mobile radio and Beidou RDSS System applications. It can be used in Class AB/B and Class C for all typical modulation formats.



DFN 5*6-8L

Typical Performance Over 1615MHz (T_c=25°C)

Table1. (Test in Innotion Fixture): VDD=12V, I_{DQ}=100mA, CW.

Frequency (MHz)	Gain (dB)	P _{sat} (W)	Eff@ P _{sat} (%)
1615	15	15	60

Capable of Handling 10:1 VSWR @ 12Vdc, 1615MHz, 15Watts CW Output Power for Enhanced Ruggedness applications.

Features

- High Efficiency and Linear Gain Operation
- Integrated ESD Protection, Class2 (HBM)
- Excellent Thermal Stability and Excellent Ruggedness
- Plastic Package for General Use

Table2. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	+40	Vdc
Gate-Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+12	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table3. Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
DC Characteristics						
Zero Gate Threshold Drain Leakage Current	I_{DSS}			10	uA	$V_{DS}=26\text{ V}$, $V_{GS}=0\text{ V}$
Zero Gate Threshold Drain Leakage Current	I_{DSS}			1	uA	$V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$
Gate--Source Leakage Current	I_{GSS}			1	uA	$V_{DS}=0\text{ V}$, $V_{GS}=6\text{ V}$
Gate Threshold Voltage	$V_{GS(th)}$		1.85		V	$V_{DS}=12\text{ V}$, $I_D=250\text{ uA}$
Gate Quiescent Voltage	$V_{GS(Q)}$		2.68		V	$V_{DD}=12\text{ V}$, $I_D=100\text{ mA}$
RF Characteristics¹ ($T_c=25^\circ\text{C}$, $F_0=1615\text{ MHz}$ unless otherwise noted)						
Saturated Output Power	P_{sat}		15		W	
Drain Efficiency@Psat,1615MHz	Eff		60		%	
Power Gain	G_P		15		dB	
Input Return Loss	I_{RL}		-10		dB	

Note:

1. Measured in INNOTION Test Fixture, 50ohm System, $V_{DD}=12\text{ V}$, $I_{DQ}=100\text{ mA}$, CW Signal Measurements.

Table 4. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^\circ\text{C}$, $T_J=200^\circ\text{C}$, DC test	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$

Table 5. Pin Description

Pin No.	Symbol	Description
1-4	Gate	RF input,
5-8	Drain	RF Output
EP	Source	The bottom exposed pad is the RF ground. For best thermal dissipation

Typical Performance

Bias: VDD=12V, IDQ=100mA, PulseWidth=20us, Dutycycle=10%)

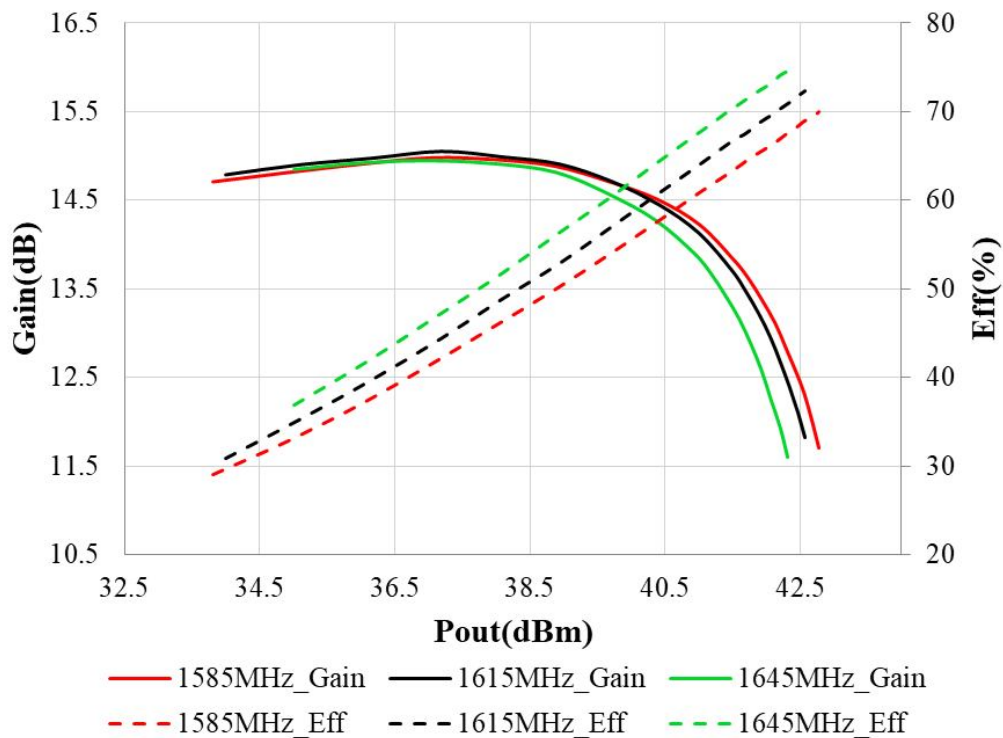


figure1. YP161515T Power sweep

Bias: YP161515T, VDD=12V, IDQ=100mA; YP163038, VCC=5V, VR=2.5V

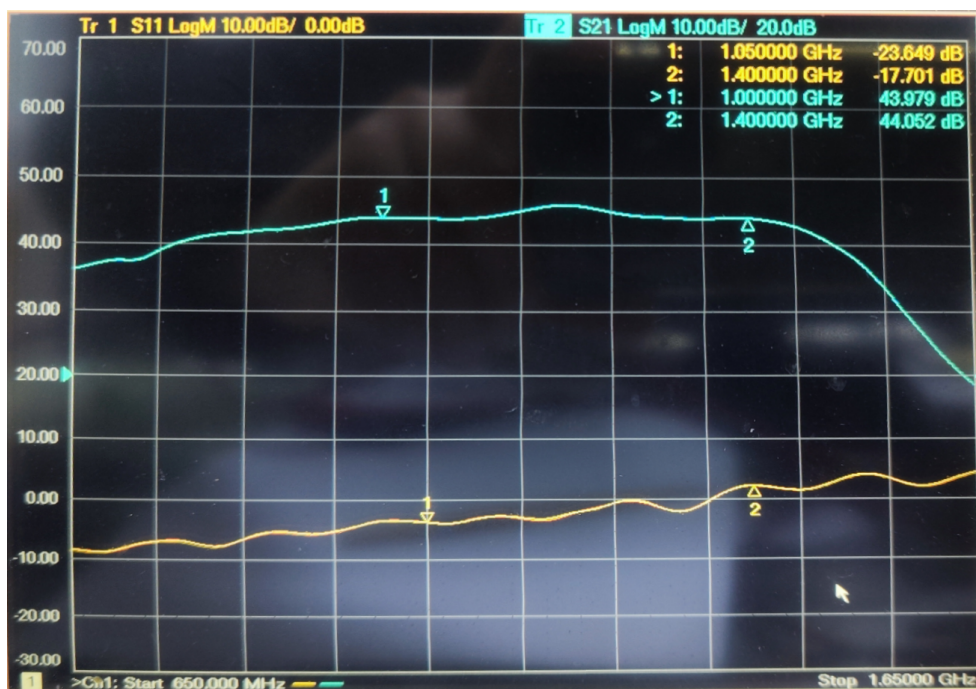
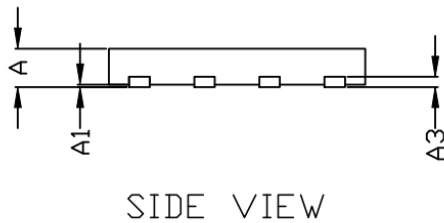
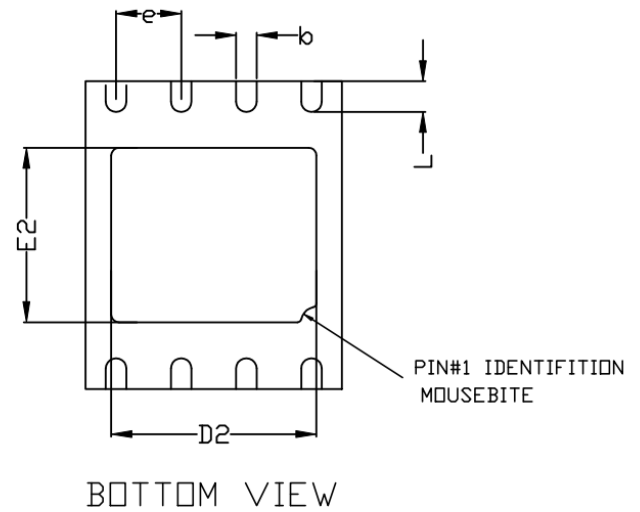
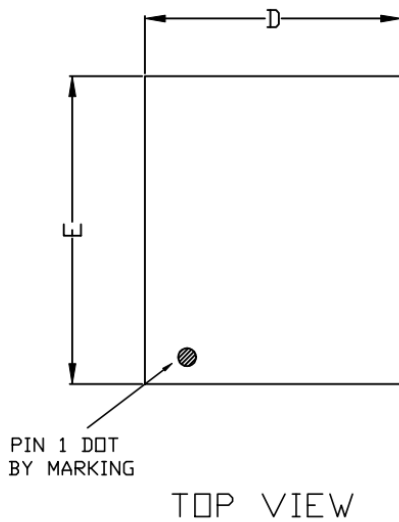


figure2. S21&S11 of YP163038+YP161515T

Packaging Diagram



COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF.		
D	4.95	5.00	5.05
E	5.95	6.00	6.05
D2	3.85	4.00	4.10
E2	3.25	3.40	3.50
b	0.35	0.40	0.45
L	0.50	0.60	0.70
e	1.27 BSC		

PIN 1 - PIN 4 : Gate
PIN 5 - PIN 8 : Drain
PIN 9(Pkg Base) : GND