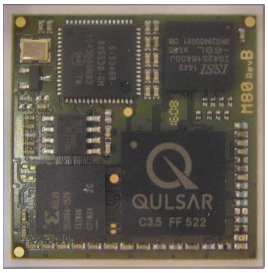
M88 Managed Clock Engine (MCE) Module



APPLICATIONS
- Mobile backhaul Carrier Ethernet
- Macro / micro eNodeB and small cell
- C-RAN BBU to RRH sync
- DOCSIS CMTS and Remote PHY
- Data center switches
- Broadband access – G.fast, xDSL and xPON
- Broadcast video genlock (SMPTE 2059)

FEATURES
- Unified full clock solution
- Synchronizes to GNSS, SyncE, BITS, PTP (IEEE 1588-2008).
- Industry-leading IEEE 1588 time & frequency recovery algorithms
- Gateway and boundary clock
- Supports one-step and two-step clock
- Telecom, power & default profiles
- Industry leading algorithm for G.8261
- Meets the requirements of:
  - ITU-T G.8261, G.8265, G.8275
  - ITU-T G.8273 T-GM, T-BC and T-TSC
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR1244, GR253 (Stratum 3/3E)
- Flexible frequency synthesis with multiple outputs
- Status monitoring: LOS, OOF, LOL
- Scalable to 128 PTP clients

BENEFITS
- Easy & rapid integration in host system
- Full clock subsystem, lower design cost
- Excellent phase noise performance
- Low power consumption
- Ultra-low jitter, network-synchronized multiple frequency outputs

Turnkey IEEE 1588-2008 and Synchronous Ethernet Network Synchronization Solution

The M88 Managed Clock Engine module combines a high precision IEEE 1588-2008 PTP packet gateway clock with Silicon Labs' Si5348 ultra-low jitter network synchronizer. The M88 is a turnkey (hardware and software) solution that provides IEEE 1588-2008 and SyncE standards-compliant phase and frequency synchronization, jitter attenuation and clock generation in a unified, small form factor design.

The M88 includes a flexible multi-sync clock manager, enabling the solution to synchronize to a wide variety of references, including GNSS (1 PPS + ToD), IEEE 1588 (PTP), SyncE and BITS, while providing simplified clock input monitoring and management. The M88 incorporates an industry-leading IEEE 1588 servo algorithm to generate the high precision synchronized clock outputs required to distribute precise and accurate timing signals for LTE, LTE-Advanced and evolving 5G transport and access networks. Typical applications include phase and frequency synchronization for wireless infrastructure and wireline broadband networks such as PON, DOCSIS, G.fast DSL and data center switches.

The M88 offers unmatched frequency synthesis, flexibility and ultra-low jitter performance. The unique design of the module enables it to accept a TCXO or OCXO with any frequency as the reference clock without degrading the jitter performance of the output clocks.

Technical Performance & Functions

The M88 is a fully managed clock module for systems implementing network-based timing. The M88 provides a PTP engine capable of operating as a IEEE 1588-2008 master, slave, boundary or gateway clock for packet-timing and a low-bandwidth, programmable network PLL for physical-layer synchronization.

Industry-leading algorithms deliver high precision PTP performance in either PTP-only or frequency-assist modes. The M88 achieves leading performance against ITU-T G.8261 and G.8273.2-compliant test suites.

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M88 MCE Module

Multi-sync & Algorithms

The M88 combines clock generation, digital oscillator control, input monitoring, management and packet timing (PTP / IEEE 1588) with advanced servo algorithms. This enables the host system to provide multiple low-jitter (low phase noise) clock outputs.

Additionally, the M88 has cutting edge technology that enables it to manage multiple inputs. The ability to use multiple synchronization sources is particularly powerful in today's applications, where a host system may need to be versatile and deployable in multiple environments, for example by supporting local-GNSS, BITS/SSU and SyncE in conjunction with PTP.

System Features

- Assisted Partial Timing Support Clock (A-PTSC) G.8273.4
- Fully compliant to telecom, power & default profiles
- Telecom Boundary Clock (T-BC) ITU-T G8273.2[1]
- Multi-sync handling support
- Phase accuracy better than ±1 µs
- Fractional Frequency Offset better than 1ppb under ITU-T G.8261 test conditions [1]

Network Interface

- 2x RGMII ports
- Integrated TCP/IP stack
- IPv4 and IPv6 (PTP)

[1] ITU-T G.8261 & ITU-T-G8273.2 tests conducted at both Qulsar internal labs and 3rd party labs – details available on request and under NDA

Functional Description

Outputs

- 5x ultra-low jitter outputs from three DSPLLs
  - Programmable frequency up to 350 MHz
  - Can be locked to any reference input or derived from PTP
  - Programmable loop B/W per DSPLL: 1 mHz - 4 kHz
- Additional 5/10/20/25 MHz syntonized output
- Time outputs: 1PPS & ToD (time of day)
- IEEE 1588-2008 (PTP) Master
  - Locked to 1PPS + ToD (GNSS), frequency or PTP slave (BC mode)

Timing References (Inputs)

- 1PPS/ToD;
- Alternative 1PPS
- PTP
- Two high-speed clocks for SyncE or SDH
- Two low-speed clocks (up to 2.048 MHz)
- External oscillator (free-run operation)

ToD Format (output)

- ASCII, NMEA and China Mobile Binary format

Physical Interfaces

- 2x Gigabit Ethernet RGMII
- Configurable clock inputs/outputs
  - LVDS, LVPECL, LVCMOS, HCSL, CML
- SPI (master and slave)
- 2x Asynchronous serial (ToD and console)
- Debug port

PTP Master

- Accuracy with GPS as reference better than ±25 ns
- Supports one and two-step operation
- Message rates up to 128 packets per second
- Multicast and unicast operation

Other Features

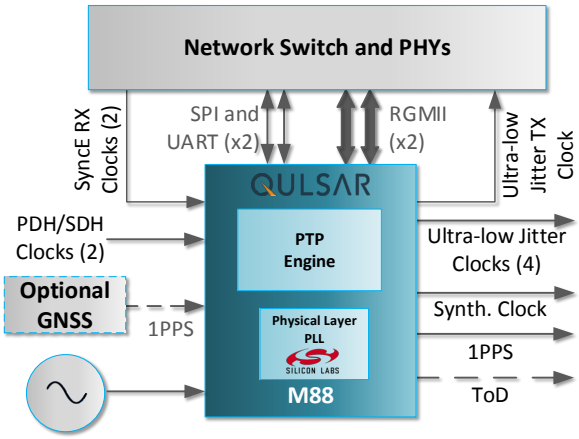
- DHCPv4 client; FTP server; TELNET server; SSH server; serial terminal
- Remote firmware upgrade
- Command line interface configuration (Telnet, SSH or serial port terminal)

Operating Specifications

- Supply: 3.3V, 1.8V & 1.2V +/- 5%
- Operating temperature: -40°C to 85°C
- RoHS-6 & WEEE compliant
- Low power dissipation: 1.1W (typical)

Physical Specifications

- Package: LGA-144
- Size: 29.2 mm X 29.2mm



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