

Product Spec

Motherboard

RB-Q370SC V1.0

Prepared by : Peter

Date: 2021/06/11

Shenzhen RealBom Intelligent Co., LTD

CONTROLLED FILE

Revision History			
Revision	Date	Description	Author
V1.0	2021/06/11	First release	Peter



Specifications

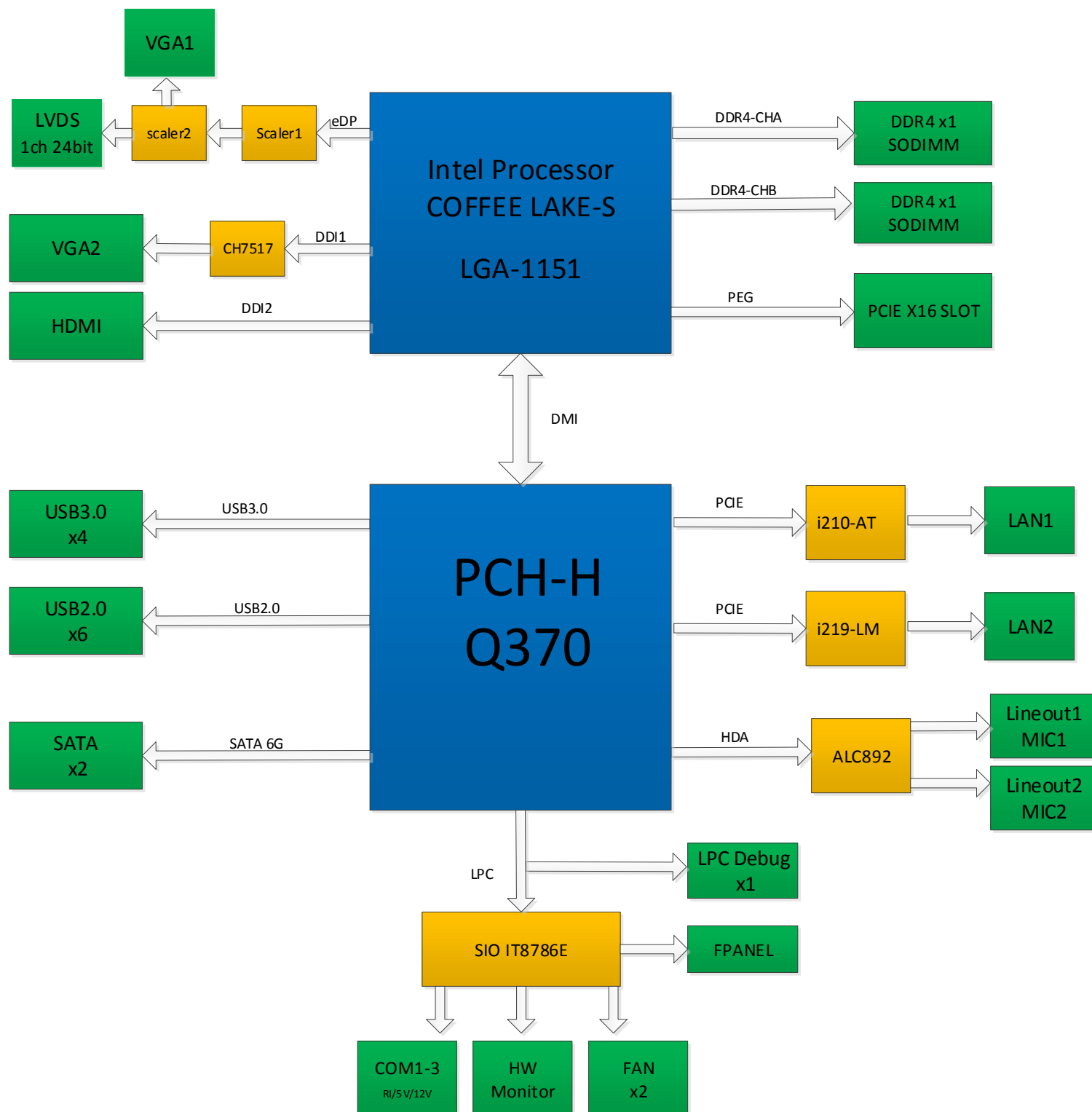
Features

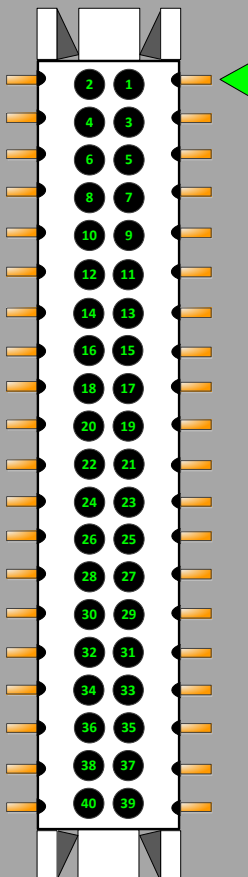
- *Intel Coffee lake-S ,Chipset Q370,TDP 65W CPU
- *Support Two channel DDR4 SODIMM
- *Support displays LVDS/VGA1+VGA2+HDMI
- *Support 2x 10/100/1000M LAN adapter
- *Support 4 x USB3.1 +6xUSB2.0
- *Support 3 x COMs
- *Support 2 x SATA
- *Support win10/Fedora
- *Support AMT/TXT Technology

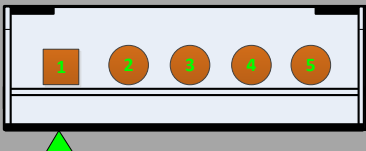
Application Industry

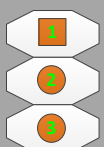
Lottery industry

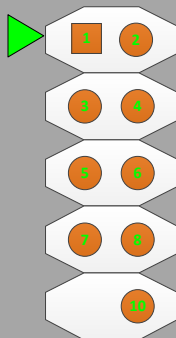
CPU	CPU	Intel Coffee lake-S LGA1151 8th/9th gen CPU, TDP 65W, G5400/i7-8700/i5-8500
	Instruction Set	64bit
CHIPSET	PCH	Q370
Memory	Type	DDR4 SODIMM
	Channel	2
	Memory Size	64GB
Audio	ALC892 HD Audio	X2 LINEOUT1+MIC1 , LINEOUT2+MIC2
Ethernet	LAN	X2 10/100/1000M LAN, 1*i210-AT, 1*i219-LM
Internal Connector	LVDS	X1 LVDS CONN(1CH 24BIT)
	SATA	X2 SATA (support DOM Power supply)
	USB2.0	X5 USB2.0 heder
	AUDIO	X1 LINEOUT2+MIC2 Header
	COM	X1 RS232 (support Pin9 0V/5V/12V jump select)
	PCIE slot	X1 PCI16X Slot
	FPANEL	X1 PWRON/RESET/PWRLED/HDDLED
	FAN	X1 CPUFAN+X1 SYSFAN
	SSD	X1 M.2 NVME (PCIEX4) SSD
	GPIO	X1 GPIO wafer
I/O	VGA	X2 VGA1+VGA2 (VGA1 clone LVDS)
	HDMI	X1 Port
	USB	X4 USB3.1 Port + X1 USB2.0 Port
	COM	X2 RS232 (support Pin9 0V/5V/12V jump select)
	RJ45	X2 Port
	AUDIO	X1 LINEOUT1+MIC1 Port
BIOS	Vender	AMI
	ACPI	Supported
Power	POWER Brick	ATX4P+ATX20P
Dimensions	PCB	177mm*175mm
Requirements Environment	Operation	-10℃~+60℃, 10%~95% RTH
	Storage	-40℃~+85℃, 10%~95% RTH

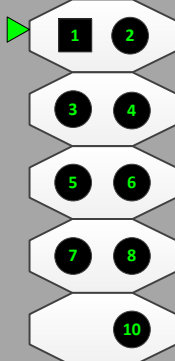


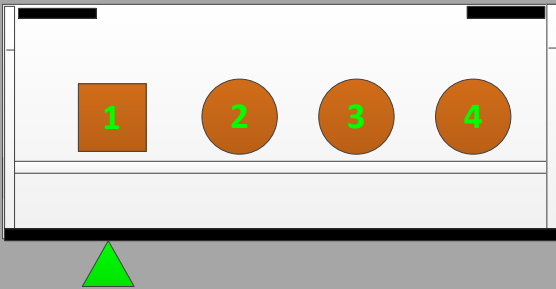
LVDS	LVDS																																																																																			
PIN Define		<table><tr><td>1</td><td>LCD_VDD</td><td>2</td><td>LCD_VDD</td></tr><tr><td>3</td><td>GND</td><td>4</td><td>GND</td></tr><tr><td>5</td><td>LCD_VDD</td><td>6</td><td>LCD_VDD</td></tr><tr><td>7</td><td>LVDS_D0-</td><td>8</td><td>NA</td></tr><tr><td>9</td><td>LVDS_D0+</td><td>10</td><td>NA</td></tr><tr><td>11</td><td>GND</td><td>12</td><td>GND</td></tr><tr><td>13</td><td>LVDS_D1-</td><td>14</td><td>NA</td></tr><tr><td>15</td><td>LVDS_D1+</td><td>16</td><td>NA</td></tr><tr><td>17</td><td>GND</td><td>18</td><td>GND</td></tr><tr><td>19</td><td>LVDS_D2-</td><td>20</td><td>NA</td></tr><tr><td>21</td><td>LVDS_D2+</td><td>22</td><td>NA</td></tr><tr><td>23</td><td>GND</td><td>24</td><td>GND</td></tr><tr><td>25</td><td>LVDS_CLK1-</td><td>26</td><td>NA</td></tr><tr><td>27</td><td>LVDS_CLK1+</td><td>28</td><td>NA</td></tr><tr><td>29</td><td>GND</td><td>30</td><td>GND</td></tr><tr><td>31</td><td>NA</td><td>32</td><td>NA</td></tr><tr><td>33</td><td>GND</td><td>34</td><td>GND</td></tr><tr><td>35</td><td>LVDS_D3-</td><td>36</td><td>NA</td></tr><tr><td>37</td><td>LVDS_D3+</td><td>38</td><td>NA</td></tr><tr><td>39</td><td>GND</td><td>40</td><td>NA</td></tr></table>			1	LCD_VDD	2	LCD_VDD	3	GND	4	GND	5	LCD_VDD	6	LCD_VDD	7	LVDS_D0-	8	NA	9	LVDS_D0+	10	NA	11	GND	12	GND	13	LVDS_D1-	14	NA	15	LVDS_D1+	16	NA	17	GND	18	GND	19	LVDS_D2-	20	NA	21	LVDS_D2+	22	NA	23	GND	24	GND	25	LVDS_CLK1-	26	NA	27	LVDS_CLK1+	28	NA	29	GND	30	GND	31	NA	32	NA	33	GND	34	GND	35	LVDS_D3-	36	NA	37	LVDS_D3+	38	NA	39	GND	40	NA
	1	LCD_VDD	2	LCD_VDD																																																																																
	3	GND	4	GND																																																																																
	5	LCD_VDD	6	LCD_VDD																																																																																
	7	LVDS_D0-	8	NA																																																																																
	9	LVDS_D0+	10	NA																																																																																
	11	GND	12	GND																																																																																
	13	LVDS_D1-	14	NA																																																																																
	15	LVDS_D1+	16	NA																																																																																
	17	GND	18	GND																																																																																
	19	LVDS_D2-	20	NA																																																																																
	21	LVDS_D2+	22	NA																																																																																
	23	GND	24	GND																																																																																
	25	LVDS_CLK1-	26	NA																																																																																
	27	LVDS_CLK1+	28	NA																																																																																
29	GND	30	GND																																																																																	
31	NA	32	NA																																																																																	
33	GND	34	GND																																																																																	
35	LVDS_D3-	36	NA																																																																																	
37	LVDS_D3+	38	NA																																																																																	
39	GND	40	NA																																																																																	
Type	2x20 PH=0.15mm																																																																																			

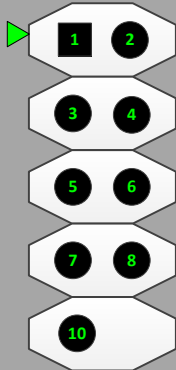
IVCN	LVDS Backlight Power and control												
PIN Define		<table><tr><td>1</td><td>+V12S</td></tr><tr><td>2</td><td>GND</td></tr><tr><td>3</td><td>BKLT_ON</td></tr><tr><td>4</td><td>BKLT_PWM</td></tr><tr><td>5</td><td>+V5S</td></tr></table>	1	+V12S	2	GND	3	BKLT_ON	4	BKLT_PWM	5	+V5S	
1	+V12S												
2	GND												
3	BKLT_ON												
4	BKLT_PWM												
5	+V5S												
Type	1X5 Header Box, PH=2.54mm												

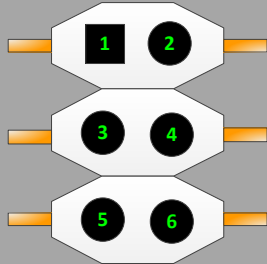
JLV	LVDS Power SELECT						
PIN Define		<table><tr><td>1-2</td><td>LCD_VDD =3.3V</td></tr><tr><td>2-3</td><td>LCD_VDD =5V</td></tr></table>	1-2	LCD_VDD =3.3V	2-3	LCD_VDD =5V	
1-2	LCD_VDD =3.3V						
2-3	LCD_VDD =5V						
Type	1X3 Header, PH=2.0mm						
Memo	Default Setting: JLV (1-2)						

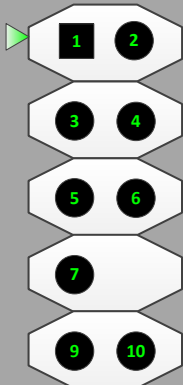
F_PANEL	LED and SYSTEM function header																				
PIN Define	 <table><tr><td>1</td><td>PWR_ON+</td><td>2</td><td>HDD_LED+</td></tr><tr><td>3</td><td>PWR_ON-</td><td>4</td><td>HDD_LED-</td></tr><tr><td>5</td><td>SYS_RESET+</td><td>6</td><td>PWR_LED+</td></tr><tr><td>7</td><td>SYS_RESET-</td><td>8</td><td>PWR_LED-</td></tr><tr><td>9</td><td></td><td>10</td><td>GND</td></tr></table>	1	PWR_ON+	2	HDD_LED+	3	PWR_ON-	4	HDD_LED-	5	SYS_RESET+	6	PWR_LED+	7	SYS_RESET-	8	PWR_LED-	9		10	GND
1	PWR_ON+	2	HDD_LED+																		
3	PWR_ON-	4	HDD_LED-																		
5	SYS_RESET+	6	PWR_LED+																		
7	SYS_RESET-	8	PWR_LED-																		
9		10	GND																		
Type	2X5 DuPont Header PH=2.5mm																				

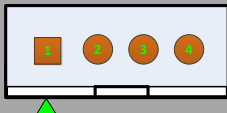
JUSB1/2	USB2.0 Header																				
PIN Define	 <table><tr><td>1</td><td>VBUS</td><td>2</td><td>VBUS</td></tr><tr><td>3</td><td>D0-</td><td>4</td><td>D1-</td></tr><tr><td>5</td><td>D0+</td><td>6</td><td>D1+</td></tr><tr><td>7</td><td>GND</td><td>8</td><td>GND</td></tr><tr><td>9</td><td>NC</td><td>10</td><td>GND</td></tr></table>	1	VBUS	2	VBUS	3	D0-	4	D1-	5	D0+	6	D1+	7	GND	8	GND	9	NC	10	GND
1	VBUS	2	VBUS																		
3	D0-	4	D1-																		
5	D0+	6	D1+																		
7	GND	8	GND																		
9	NC	10	GND																		
Type	2x5 DuPont Header, PIN9 NC, PH=2.5mm																				

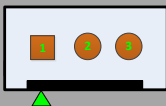
JUSB3	USB2.0 wafer								
PIN Define	 <table border="1"> <tr> <td>1</td><td>VBUS</td></tr> <tr> <td>2</td><td>D-</td></tr> <tr> <td>3</td><td>D+</td></tr> <tr> <td>4</td><td>GND</td></tr> </table>	1	VBUS	2	D-	3	D+	4	GND
1	VBUS								
2	D-								
3	D+								
4	GND								
Type	1X4 Wafer, PH=2.5mm								

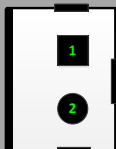
COM3	COM header RS232																				
PIN Define	 <table><tr><td>1</td><td>DCD</td><td>2</td><td>RXD</td></tr><tr><td>3</td><td>TXD</td><td>4</td><td>DTR</td></tr><tr><td>5</td><td>GND</td><td>6</td><td>DSR</td></tr><tr><td>7</td><td>RTS</td><td>8</td><td>CTS</td></tr><tr><td>9</td><td>RI_MUX</td><td>10</td><td>NC</td></tr></table>	1	DCD	2	RXD	3	TXD	4	DTR	5	GND	6	DSR	7	RTS	8	CTS	9	RI_MUX	10	NC
1	DCD	2	RXD																		
3	TXD	4	DTR																		
5	GND	6	DSR																		
7	RTS	8	CTS																		
9	RI_MUX	10	NC																		
Type	2X5 Header PH=2.5 mm																				

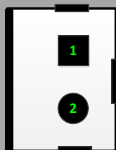
JC1/2/3	COM1-3 Pin power select												
PIN Define	 <table><tr><td>1</td><td>RI</td><td>2</td><td>COM1. PIN9</td></tr><tr><td>3</td><td>5V</td><td>4</td><td>COM1. PIN9</td></tr><tr><td>5</td><td>12V</td><td>6</td><td>COM1. PIN9</td></tr></table>	1	RI	2	COM1. PIN9	3	5V	4	COM1. PIN9	5	12V	6	COM1. PIN9
1	RI	2	COM1. PIN9										
3	5V	4	COM1. PIN9										
5	12V	6	COM1. PIN9										
Type	2x3 DuPont Header, PH=2.0mm												
Memo	Default setting:1-2												

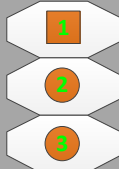
F_AUDIO	AUDIO Header				
PIN Define					
		1	MIC2_L	2	AGND
		3	MIC2_R	4	3.3V
		5	LINE2_R	6	MIC2_DET
		7	AGND	8	NC
		9	LINE2_L	10	LINE2_DET
Type	2x5 DuPont Header, PH=2.5mm				

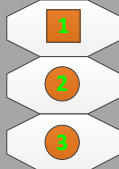
FAN	CPU FAN		
PIN Define		1	FAN_CTL
		2	FAN_TAC
		3	+V12S
		4	GND
Type	1X4 DuPont Header, PH=2.54mm		

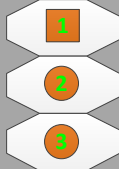
SYS_FAN	System Fan Power and sense								
PIN Define		<table><tr><td>1</td><td>GND</td></tr><tr><td>2</td><td>+V12S</td></tr><tr><td>3</td><td>FAN_TAC</td></tr></table>	1	GND	2	+V12S	3	FAN_TAC	
1	GND								
2	+V12S								
3	FAN_TAC								
Type	1X3 DuPont Header, PH=2.54mm								

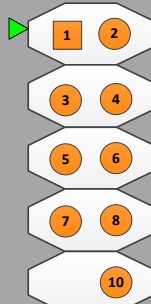
SATAPWR1/2	SATA Power					
PIN Define		<table><tr><td>1</td><td>5V</td></tr><tr><td>2</td><td>GND</td></tr></table>	1	5V	2	GND
1	5V					
2	GND					
Type	1X2 WAFER, PH=2.0mm					

J1	GPIO WAFER						
PIN Define		<table><tr><td>1</td><td>GND</td></tr><tr><td>2</td><td>GPIO</td></tr></table>	1	GND	2	GPIO	
1	GND						
2	GPIO						
Type	1X2 WAFER, PH=2.0mm						

JCOMS	CLEAR CMOS header					
PIN Define		<table><tr><td>1-2</td><td>Normal</td></tr><tr><td>2-3</td><td>Clear cmos</td></tr></table>	1-2	Normal	2-3	Clear cmos
1-2	Normal					
2-3	Clear cmos					
Type	1X3 DuPont Header, PH=2.5mm					
Memo	Default Setting: JCmos(1-2)					

JME	ME fucktion header					
PIN Define		<table><tr><td>1-2</td><td>Normal</td></tr><tr><td>2-3</td><td>Override ME</td></tr></table>	1-2	Normal	2-3	Override ME
1-2	Normal					
2-3	Override ME					
Type	1X3 DuPont Header, PH=2.5mm					
Memo	Default Setting: N/A					

JVGA1	VGA2 CH7517 FW UPDATE header(DEBUG OPTION)							
PIN Define		<table><tr><td>1</td><td>SPC</td></tr><tr><td>2</td><td>SPD</td></tr><tr><td>3</td><td>GND</td></tr></table>	1	SPC	2	SPD	3	GND
1	SPC							
2	SPD							
3	GND							
Type	1X3 DuPont Header, PH=2.0mm							

DEBUG	LPC DEBUG																							
PIN Define	 <table><tr><td>1</td><td>LAD3</td><td>2</td><td>25M_CLK</td></tr><tr><td>3</td><td>LAD2</td><td>4</td><td>LFRAME#</td></tr><tr><td>5</td><td>LAD1</td><td>6</td><td>LESET#</td></tr><tr><td>7</td><td>LAD0</td><td>8</td><td>GND</td></tr><tr><td>9</td><td>NC</td><td>10</td><td>+3.3V</td></tr></table>				1	LAD3	2	25M_CLK	3	LAD2	4	LFRAME#	5	LAD1	6	LESET#	7	LAD0	8	GND	9	NC	10	+3.3V
1	LAD3	2	25M_CLK																					
3	LAD2	4	LFRAME#																					
5	LAD1	6	LESET#																					
7	LAD0	8	GND																					
9	NC	10	+3.3V																					
Type	2x5 DuPont Header, PIN9 NC, PH=2.0mm																							
Memo	For Debug only																							