

Product Spec

Motherboard

RB-J1900BW V1.0

Prepared by : Ken

Date: 2017/10/31

Approved by: Peter

Date: 2017/10/31

Revision History			
Revision	Date	Description	Author
V1.0	2017/10/31	First release	KEN



Specifications

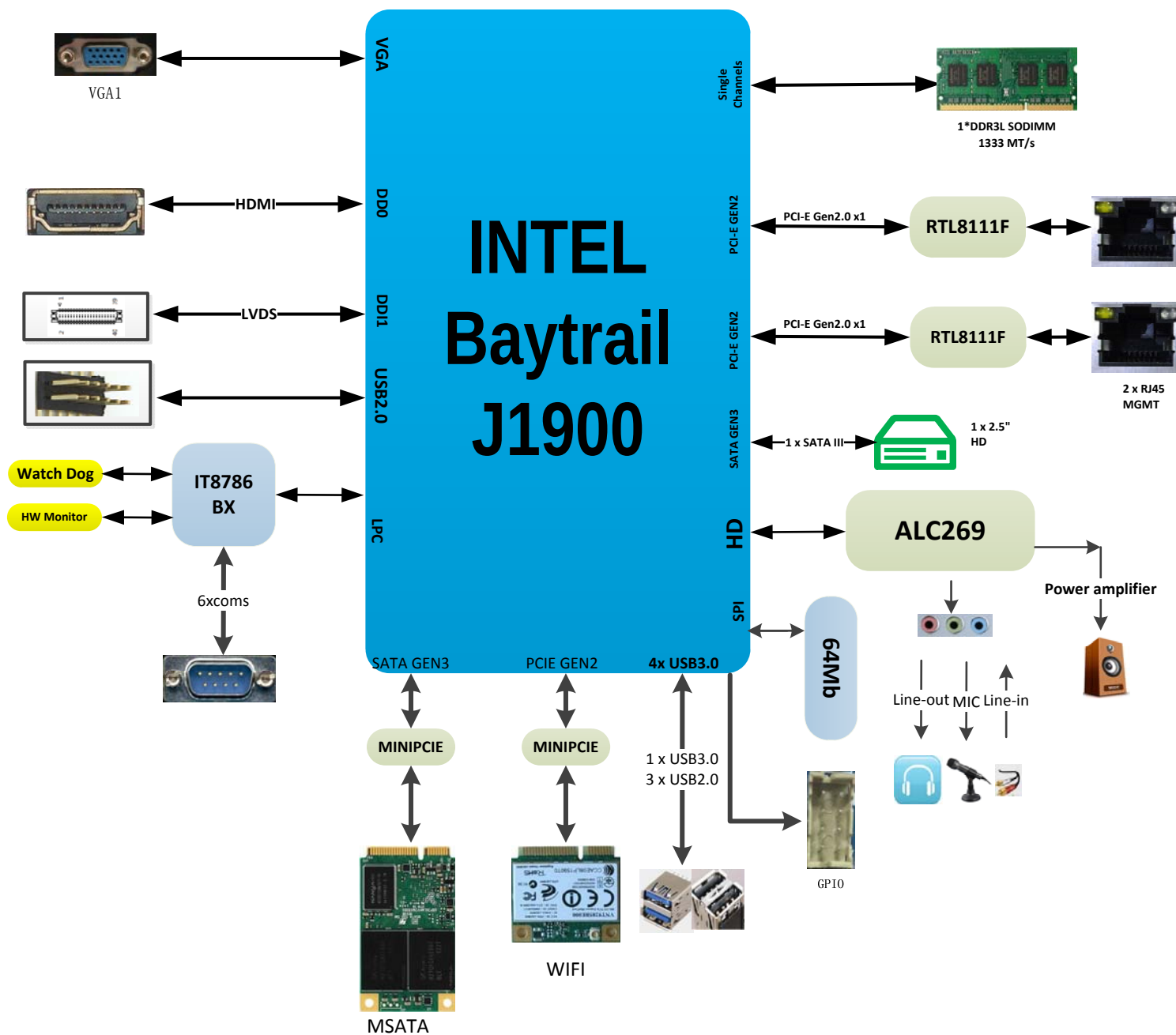
Features

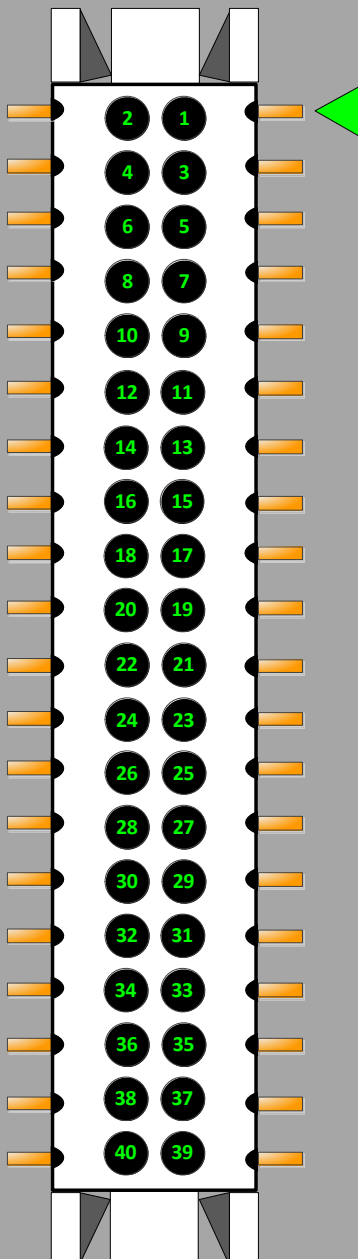
- *Intel Baytrail Platform, J1900 CPU, 2.0GHz, 4Cores
- *Supports 2 x Display VGA+HDMI+LVDS,
- *Supports 2x 10/100/1000M LAN adapter
- *Support 11 x USB2.0, 1 x USB3.0
- *Support 6 x COMs, 1 x SATAII, 1 x MSATA , 1 x WIFI ,1xPCIEX1,1xLPT
- *Support HD Audio , 1 x line out, 1 x line in,1x MIC,4ohm &2w Power amplifier
- *One 204-pin SODIMM up to 8GB, DDR3L 1333 MHz

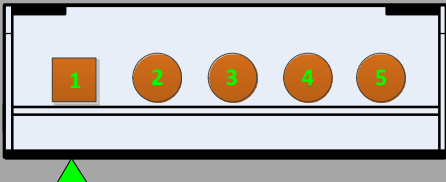
Application Industry

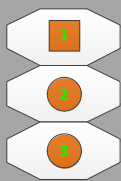
Medical industry.Traffic industry, Advertising Machine,Financial industry,

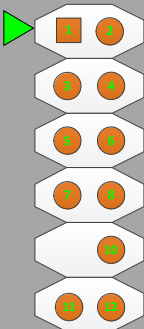
CPU	CPU	Intel Baytrail J1900 2 GHz- 2.4 GHz
	Instruction Set	64bit
	Lithography	22nm
Memory	Type	SODIMM DDR3L No ECC ,Supoort 1333 MHz
	Channel	Single
	Max Memory Size	8GB
Graphics	Graphics	Intel HD Graphics
	Displays Supported	3 Display Port VGA& HDMI & LVDS
Audio	ALC269 HD Audio	x1 line out,、x1 line in 、x1 MIC、4ohm&2W Power amplifier
Ethernet	RTL8111F	x2 10/100/1000M BASET LAN
Internal Connector	MSATA	x1 MINIPCIIE
	SATA	x1 7PIN SATA
	WIFI	x1 Half length MINIPCIIE
	LVDS	x1 2x20 Header Box
	PCIE1X	x1 PCIE1X
	COM	x3 COM4-COM6 (RS232) 2x5 Header Box,Powered 5V(Optional)
	USB	x2 2x5 DuPont Header (support 4* USB2.0)
	USB	x1 2x6 DuPont Header (support 2* USB2.0 and I2C)
	LPT	x1 2x13 DuPont Header
	PS2	x1 2x4 DuPont Header
	GPIO	x1 2X6 DuPont Header ,8*independent Programing GPIO
I/O	Input DC connector	x2 1xDC jack ,1xATX Power 4Pin connector
	COM	x3 DB9 Com1-2 Powered 5V/12V(Optional), Com3 Powered 5V (Optional)
	USB	x4 1xPorts USB3.0 and 3xUSB2.0
	RJ45	x2 Single RJ45
	Aduio	x1 Suport Line out,Line in,mic
	VGA	x1 Standard VGA
	HDMI	x1 Standard HDMI
BIOS	Vender	AMI
	ACPI	Supported
Power	POWER Brick	9V-24V DC POWER Brick
Dimensions	PCB	170*170MM
Requirements Environment	Operation	-15℃~+50℃ , 10%~95% RTH
	Storage	-40℃~+70℃ , 10%~95% RTH

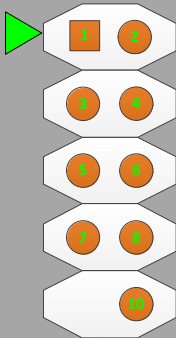


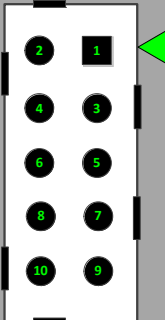
LVDS	LVDS																																																																															
PIN Define																																																																																
	<table><tr><td>1</td><td>LCD_VDD</td><td>2</td><td>LCD_VDD</td></tr><tr><td>3</td><td>LCD_VDD</td><td>4</td><td>LCD_VDD</td></tr><tr><td>5</td><td>BKLT_ON</td><td>6</td><td>BKLT_CTL</td></tr><tr><td>7</td><td>GND</td><td>8</td><td>GND</td></tr><tr><td>9</td><td>LVDS_D1+</td><td>10</td><td>LVDS_D0+</td></tr><tr><td>11</td><td>LVDS_D1-</td><td>12</td><td>LVDS_D0-</td></tr><tr><td>13</td><td>GND</td><td>14</td><td>GND</td></tr><tr><td>15</td><td>LVDS_D3+</td><td>16</td><td>LVDS_D2+</td></tr><tr><td>17</td><td>LVDS_D3-</td><td>18</td><td>LVDS_D2-</td></tr><tr><td>19</td><td>GND</td><td>20</td><td>GND</td></tr><tr><td>21</td><td>LVDS_D5+</td><td>22</td><td>LVDS_D4+</td></tr><tr><td>23</td><td>LVDS_D5-</td><td>24</td><td>LVDS_D4-</td></tr><tr><td>25</td><td>GND</td><td>26</td><td>GND</td></tr><tr><td>27</td><td>LVDS_D7+</td><td>28</td><td>LVDS_D6+</td></tr><tr><td>29</td><td>LVDS_D7-</td><td>30</td><td>LVDS_D6-</td></tr><tr><td>31</td><td>GND</td><td>32</td><td>GND</td></tr><tr><td>33</td><td>LVDS_CLK2+</td><td>34</td><td>LVDS_CLK1+</td></tr><tr><td>35</td><td>LVDS_CLK2-</td><td>36</td><td>LVDS_CLK1-</td></tr><tr><td>37</td><td>GND</td><td>38</td><td>GND</td></tr><tr><td>39</td><td>+V12S</td><td>40</td><td>+V12S</td></tr></table>	1	LCD_VDD	2	LCD_VDD	3	LCD_VDD	4	LCD_VDD	5	BKLT_ON	6	BKLT_CTL	7	GND	8	GND	9	LVDS_D1+	10	LVDS_D0+	11	LVDS_D1-	12	LVDS_D0-	13	GND	14	GND	15	LVDS_D3+	16	LVDS_D2+	17	LVDS_D3-	18	LVDS_D2-	19	GND	20	GND	21	LVDS_D5+	22	LVDS_D4+	23	LVDS_D5-	24	LVDS_D4-	25	GND	26	GND	27	LVDS_D7+	28	LVDS_D6+	29	LVDS_D7-	30	LVDS_D6-	31	GND	32	GND	33	LVDS_CLK2+	34	LVDS_CLK1+	35	LVDS_CLK2-	36	LVDS_CLK1-	37	GND	38	GND	39	+V12S	40
1	LCD_VDD	2	LCD_VDD																																																																													
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7	GND	8	GND																																																																													
9	LVDS_D1+	10	LVDS_D0+																																																																													
11	LVDS_D1-	12	LVDS_D0-																																																																													
13	GND	14	GND																																																																													
15	LVDS_D3+	16	LVDS_D2+																																																																													
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19	GND	20	GND																																																																													
21	LVDS_D5+	22	LVDS_D4+																																																																													
23	LVDS_D5-	24	LVDS_D4-																																																																													
25	GND	26	GND																																																																													
27	LVDS_D7+	28	LVDS_D6+																																																																													
29	LVDS_D7-	30	LVDS_D6-																																																																													
31	GND	32	GND																																																																													
33	LVDS_CLK2+	34	LVDS_CLK1+																																																																													
35	LVDS_CLK2-	36	LVDS_CLK1-																																																																													
37	GND	38	GND																																																																													
39	+V12S	40	+V12S																																																																													
Type	2x20 PH=0.15mm																																																																															

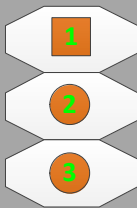
VP1	LVDS Power and Control										
PIN Define	 <table><tr><td>1</td><td>+V12S</td></tr><tr><td>2</td><td>GND</td></tr><tr><td>3</td><td>LVDS BKLT_ON</td></tr><tr><td>4</td><td>LVDS_BKLT_PWM</td></tr><tr><td>5</td><td>+V5S</td></tr></table>	1	+V12S	2	GND	3	LVDS BKLT_ON	4	LVDS_BKLT_PWM	5	+V5S
1	+V12S										
2	GND										
3	LVDS BKLT_ON										
4	LVDS_BKLT_PWM										
5	+V5S										
Type	1X5 Header Box, PH=2.54mm										

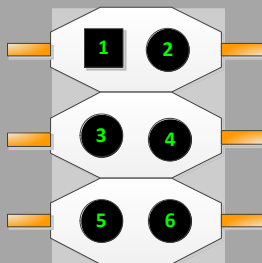
JLV	LVDS Power option						
PIN Define	 <table border="1"> <tr> <td>1</td><td>+V3.3S</td></tr> <tr> <td>2</td><td>LCD_VDD</td></tr> <tr> <td>3</td><td>+V5S</td></tr> </table>	1	+V3.3S	2	LCD_VDD	3	+V5S
1	+V3.3S						
2	LCD_VDD						
3	+V5S						
Type	1X3 DuPont Header, PH=2.54mm						
Memo	Default Setting: JLV (1-2)						

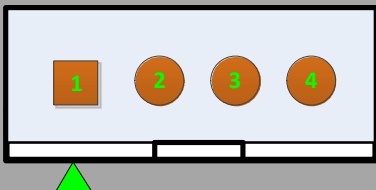
JUSB	JUSB3																								
PIN Define	 <table><tr><td>1</td><td>VCC</td><td>2</td><td>VCC</td></tr><tr><td>3</td><td>Data1-</td><td>4</td><td>Data2-</td></tr><tr><td>5</td><td>Data1+</td><td>6</td><td>Data2+</td></tr><tr><td>7</td><td>GND</td><td>8</td><td>GND</td></tr><tr><td>9</td><td></td><td>10</td><td>GND</td></tr><tr><td>11</td><td>I2C_DATA</td><td>12</td><td>I2C_CLK</td></tr></table>	1	VCC	2	VCC	3	Data1-	4	Data2-	5	Data1+	6	Data2+	7	GND	8	GND	9		10	GND	11	I2C_DATA	12	I2C_CLK
1	VCC	2	VCC																						
3	Data1-	4	Data2-																						
5	Data1+	6	Data2+																						
7	GND	8	GND																						
9		10	GND																						
11	I2C_DATA	12	I2C_CLK																						
Type	2X6 DuPont Header PH=2.0 mm																								

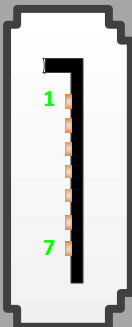
JUSB	JUSB(1-2、 4)																				
PIN Define	 <table><tr><td>1</td><td>VCC</td><td>2</td><td>VCC</td></tr><tr><td>3</td><td>Data1-</td><td>4</td><td>Data2-</td></tr><tr><td>5</td><td>Data1+</td><td>6</td><td>Data2+</td></tr><tr><td>7</td><td>GND</td><td>8</td><td>GND</td></tr><tr><td>9</td><td></td><td>10</td><td>GND</td></tr></table>	1	VCC	2	VCC	3	Data1-	4	Data2-	5	Data1+	6	Data2+	7	GND	8	GND	9		10	GND
1	VCC	2	VCC																		
3	Data1-	4	Data2-																		
5	Data1+	6	Data2+																		
7	GND	8	GND																		
9		10	GND																		
Type	2X5 DuPont Header PH=2.0 mm																				

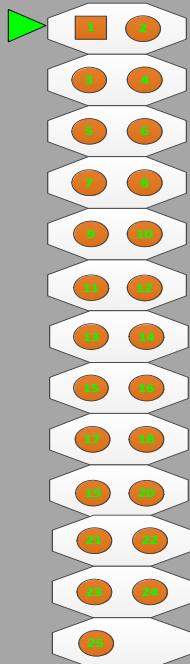
COM	COM3-COM10																							
PIN Define			<table><tr><td>1</td><td>DCD</td><td>2</td><td>RXD</td></tr><tr><td>3</td><td>TXD</td><td>4</td><td>DTR</td></tr><tr><td>5</td><td>GND</td><td>6</td><td>DSR</td></tr><tr><td>7</td><td>RTS</td><td>8</td><td>CTS</td></tr><tr><td>9</td><td>RI_MUX</td><td>10</td><td>NC</td></tr></table>		1	DCD	2	RXD	3	TXD	4	DTR	5	GND	6	DSR	7	RTS	8	CTS	9	RI_MUX	10	NC
	1	DCD	2	RXD																				
	3	TXD	4	DTR																				
	5	GND	6	DSR																				
	7	RTS	8	CTS																				
9	RI_MUX	10	NC																					
Type	2X5 Header Box PH=2.0 mm																							

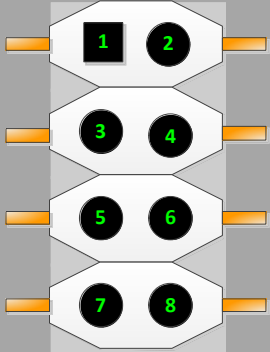
COM Power	JC3-JC6										
PIN Define	 <table border="1"> <tr><td>1</td><td>RI</td></tr> <tr><td>2</td><td>RI_MUX</td></tr> <tr><td>3</td><td>5V</td></tr> <tr><td>1-2</td><td>RI</td></tr> <tr><td>3-4</td><td>5V</td></tr> </table>	1	RI	2	RI_MUX	3	5V	1-2	RI	3-4	5V
1	RI										
2	RI_MUX										
3	5V										
1-2	RI										
3-4	5V										
Type	1X3 DuPont Header, PH=2.0mm										
Memo	Default Setting: JC3-JC6 (1-2)										

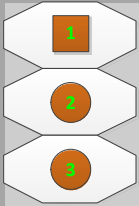
COM Power	JC1/JC2										
PIN Define	 <table><tr><td>1</td><td>5V</td><td>2</td><td rowspan="3">RI_MUX</td></tr><tr><td>3</td><td>RI</td><td>4</td></tr><tr><td>5</td><td>12V</td><td>6</td></tr></table>	1	5V	2	RI_MUX	3	RI	4	5	12V	6
1	5V	2	RI_MUX								
3	RI	4									
5	12V	6									
Type	2x3 DuPont Header, PH=2.0mm										
Memo	FOR DB9 (Pin9) com power optioan, Default Setting: JC1(3-4) JC2(3-4)										

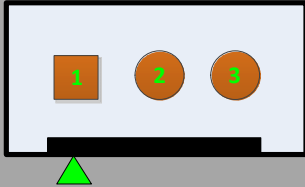
SATAPWR1	SATA POWER								
PIN Define	 <table border="1"> <tr><td>1</td><td>+V12S</td></tr> <tr><td>2</td><td>GND</td></tr> <tr><td>3</td><td>GND</td></tr> <tr><td>4</td><td>+V5S</td></tr> </table>	1	+V12S	2	GND	3	GND	4	+V5S
1	+V12S								
2	GND								
3	GND								
4	+V5S								
Type	1X4 DuPont Header, PH=2.54mm								

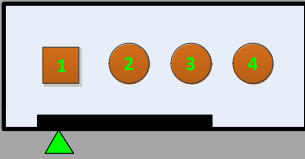
SATA	SATA1														
PIN Define	 <table border="1"> <tr><td>1</td><td>GND</td></tr> <tr><td>2</td><td>TX+</td></tr> <tr><td>3</td><td>TX-</td></tr> <tr><td>4</td><td>GND</td></tr> <tr><td>5</td><td>RX-</td></tr> <tr><td>6</td><td>RX+</td></tr> <tr><td>7</td><td>GND</td></tr> </table>	1	GND	2	TX+	3	TX-	4	GND	5	RX-	6	RX+	7	GND
1	GND														
2	TX+														
3	TX-														
4	GND														
5	RX-														
6	RX+														
7	GND														
Type	7PIN Standard SATA														

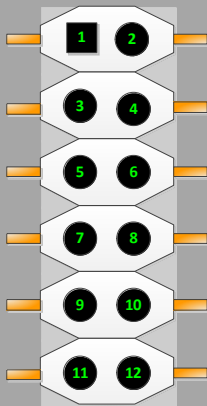
LPT	LPT																																																					
PIN Define		<table><tr><td>1</td><td>STB#</td><td>2</td><td>AFD#</td></tr><tr><td>3</td><td>PD0</td><td>4</td><td>ERR#</td></tr><tr><td>5</td><td>PD1</td><td>6</td><td>INIT#</td></tr><tr><td>7</td><td>PD2</td><td>8</td><td>SLIN#</td></tr><tr><td>9</td><td>PD3</td><td>10</td><td>GND</td></tr><tr><td>11</td><td>PD4</td><td>12</td><td>GND</td></tr><tr><td>13</td><td>PD5</td><td>14</td><td>GND</td></tr><tr><td>15</td><td>PD6</td><td>16</td><td>GND</td></tr><tr><td>17</td><td>PD7</td><td>18</td><td>GND</td></tr><tr><td>19</td><td>ACK#</td><td>20</td><td>GND</td></tr><tr><td>21</td><td>BUSY</td><td>22</td><td>GND</td></tr><tr><td>23</td><td>PE</td><td>24</td><td>GND</td></tr><tr><td>25</td><td>SLCT</td><td>26</td><td>NC</td></tr></table>	1	STB#	2	AFD#	3	PD0	4	ERR#	5	PD1	6	INIT#	7	PD2	8	SLIN#	9	PD3	10	GND	11	PD4	12	GND	13	PD5	14	GND	15	PD6	16	GND	17	PD7	18	GND	19	ACK#	20	GND	21	BUSY	22	GND	23	PE	24	GND	25	SLCT	26	NC
	1	STB#	2	AFD#																																																		
	3	PD0	4	ERR#																																																		
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	9	PD3	10	GND																																																		
	11	PD4	12	GND																																																		
	13	PD5	14	GND																																																		
	15	PD6	16	GND																																																		
	17	PD7	18	GND																																																		
	19	ACK#	20	GND																																																		
	21	BUSY	22	GND																																																		
23	PE	24	GND																																																			
25	SLCT	26	NC																																																			
Type	2X13 Header Box PH=2.0 mm																																																					

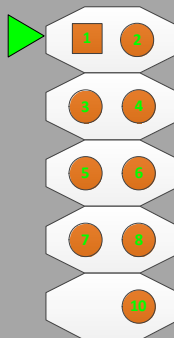
J_PS2	Ps2 header																
PIN Define	 <table><tr><td>1</td><td>KB_DATA</td><td>2</td><td>MS_DATA</td></tr><tr><td>3</td><td>KB_CLK</td><td>4</td><td>MS_CLK</td></tr><tr><td>5</td><td>GND</td><td>6</td><td>GND</td></tr><tr><td>7</td><td>+V5S</td><td>8</td><td>+V5S</td></tr></table>	1	KB_DATA	2	MS_DATA	3	KB_CLK	4	MS_CLK	5	GND	6	GND	7	+V5S	8	+V5S
1	KB_DATA	2	MS_DATA														
3	KB_CLK	4	MS_CLK														
5	GND	6	GND														
7	+V5S	8	+V5S														
Type	2x4 DuPont Header, PH=2.0mm																

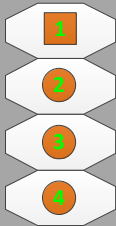
PWR_AT	AT&ATX mode option				
PIN Define	 <table border="1"> <tbody> <tr><td>1-2</td><td>ATX</td></tr> <tr><td>3-4</td><td>AT</td></tr> </tbody> </table>	1-2	ATX	3-4	AT
1-2	ATX				
3-4	AT				
Type	1X3 DuPont Header, PH=2.0mm				
Memo	Default Setting: PWR_AT(1-2)				

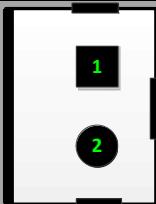
SYS_FAN	System Fan Power and sense						
PIN Define	 <table border="1"> <tr><td>1</td><td>GND</td></tr> <tr><td>2</td><td>+V12S</td></tr> <tr><td>3</td><td>FAN_TAC</td></tr> </table>	1	GND	2	+V12S	3	FAN_TAC
1	GND						
2	+V12S						
3	FAN_TAC						
Type	1X3 DuPont Header, PH=2.54mm						

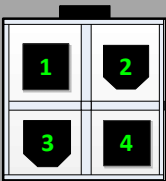
CPU_FAN	CPU FAN Power and Control								
PIN Define	 <table border="1"> <tr><td>1</td><td>GND</td></tr> <tr><td>2</td><td>+V12S</td></tr> <tr><td>3</td><td>FAN_TAC</td></tr> <tr><td>4</td><td>FAN_CTL</td></tr> </table>	1	GND	2	+V12S	3	FAN_TAC	4	FAN_CTL
1	GND								
2	+V12S								
3	FAN_TAC								
4	FAN_CTL								
Type	1X4 DuPont Header, PH=2.54mm								

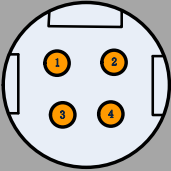
GPIO	GPIO Pin Define			
PIN Define				
	1	+V5S	2	+V12S
	3	GPIO1	4	GPIO5
	5	GPIO2	6	GPIO6
	7	GPIO3	8	GPIO7
	9	GPIO4	10	GPIO8
	11	GND	12	GND
Type	2x6 DuPont Header , PH=2.54mm			

FPNAEL	LED and SYSTEM function header																				
PIN Define	 <table><tr><td>1</td><td>PWR_ON</td><td>2</td><td>HDD_LED+</td></tr><tr><td>3</td><td>GND</td><td>4</td><td>HDD_LED-</td></tr><tr><td>5</td><td>SYS_RESET</td><td>6</td><td>PWR_LED+</td></tr><tr><td>7</td><td>GND</td><td>8</td><td>PWR_LED-</td></tr><tr><td>9</td><td></td><td>10</td><td>GND</td></tr></table>	1	PWR_ON	2	HDD_LED+	3	GND	4	HDD_LED-	5	SYS_RESET	6	PWR_LED+	7	GND	8	PWR_LED-	9		10	GND
1	PWR_ON	2	HDD_LED+																		
3	GND	4	HDD_LED-																		
5	SYS_RESET	6	PWR_LED+																		
7	GND	8	PWR_LED-																		
9		10	GND																		
Type	2X5 DuPont Header PH=2.54mm																				

JCOMS	Cmos and ME fucktion header						
PIN Define	 <table border="1"> <tr><td>1-2</td><td>Normal</td></tr> <tr><td>2-3</td><td>Clear cmos</td></tr> <tr><td>3-4</td><td>Override ME</td></tr> </table>	1-2	Normal	2-3	Clear cmos	3-4	Override ME
1-2	Normal						
2-3	Clear cmos						
3-4	Override ME						
Type	1X4 DuPont Header, PH=2.0mm						
Memo	Default Setting: JCmos(1-2)						

SPKR_L/SPKR_R	Power amplifier				
PIN Define	 <table border="1"> <tr><td>1</td><td>SPKR_L-/SPKR_R-</td></tr> <tr><td>2</td><td>SPKR_L+/SPKR_R+</td></tr> </table>	1	SPKR_L-/SPKR_R-	2	SPKR_L+/SPKR_R+
1	SPKR_L-/SPKR_R-				
2	SPKR_L+/SPKR_R+				
Type	1x2 Wafer Box PH=2.0 mm				

DC-PWR	ATX 4Pin				
PIN Define	 <table border="1"> <tr><td>1-2</td><td>DC+</td></tr> <tr><td>3-4</td><td>DC-</td></tr> </table>	1-2	DC+	3-4	DC-
1-2	DC+				
3-4	DC-				
Type	ATX Standard 4 pin connector				

DC-PWR	DC-JACK				
PIN Define	 <table border="1"> <tr><td>1/3</td><td>DC-</td></tr> <tr><td>2/4</td><td>DC+</td></tr> </table>	1/3	DC-	2/4	DC+
1/3	DC-				
2/4	DC+				
Type	DC Jack				